

ASUS CONFIDENTIAL

MODEL NAME : *Elsa*

PCB NO : ???

ASUS P/N : ???

Lanai UMA Schematics Document

uFCPGA Mobile Merom
Intel Crestline-GM + ICH8M

2007-03-19

REV :1.2(DELL: X02)

MB PCB	
Part Number	Description
DA800004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???

PCB P/N: ???

PROJECT:

REVISION

1.2

DATE: *Monday, March 19, 2007*

SHEET 1 OF 68

DESCRIPTION:

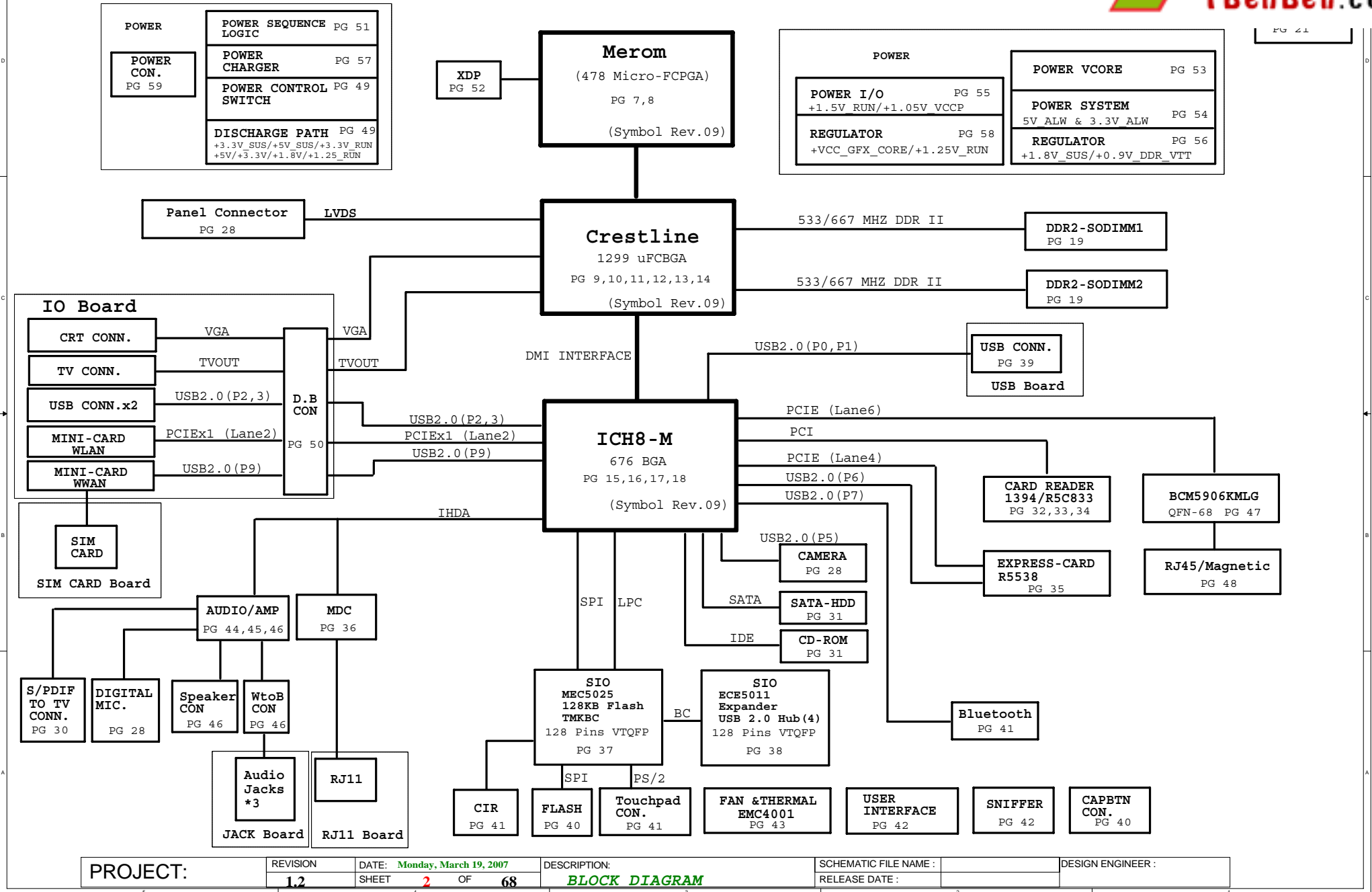
Cover Page

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RELEASE DATE :

DESIGN ENGINEER :

LANAI: UMA



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	INDEX				
1	Pg#	Description	DNI LIST	Pg#	Description
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	02	Schematic Block Diagram		64	Modem board cover page
	03	INDEX		65	RJ-11 CONN
	04	Bus connection		66	Modem board change List
	05	SMBUS BLOCK		67	USB board cover page
	06	Power Rail		68	USB PORT (SINGLE * 2)
2	07-08	CPU (Merom 、 Penryn)			
	09-14	Crestline			
	15-18	ICH8M			
	19-20	DDRII SO-DIMM(533MHz 、 667MHz)			
	21	Clock Generator (CK410M+LP)			
	22-27	BLANK PAGE			
	28	LVDS CON & Camera & DMIC			
3	29	RGB CON			
	30	TV OUT CON			
	31	SATA(HDD & CD_ROM)			
	32-34	MEDIA CARD READER / 1394 (R5C833)			
	35	PCI-Express Card			
	36	MDC CONN			
	37	EC (MEC5025)			
4	38	SIO (ECE5011)			
	39	USB PORT x 2			
	40	FLASH & RTC & CAPBTN CONN			
	41	TOUCH PAD & BT & CIR & LID			
	42	SWITCH & LED			
	43	HARDWARE MONITOR (EMC4001)			
	44-46	AUDIO CODEC & AMP			
5	47	LOM BCM5906			
	48	Magnetics and RJ-45			
	49	Power Control Switch			
	50	BtoB CON			
	51	Power Sequence Logic			
	52	XDP			
	53-59	Power Circuit			
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	61	Change List 1			
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Footprint Definition	
Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note
For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

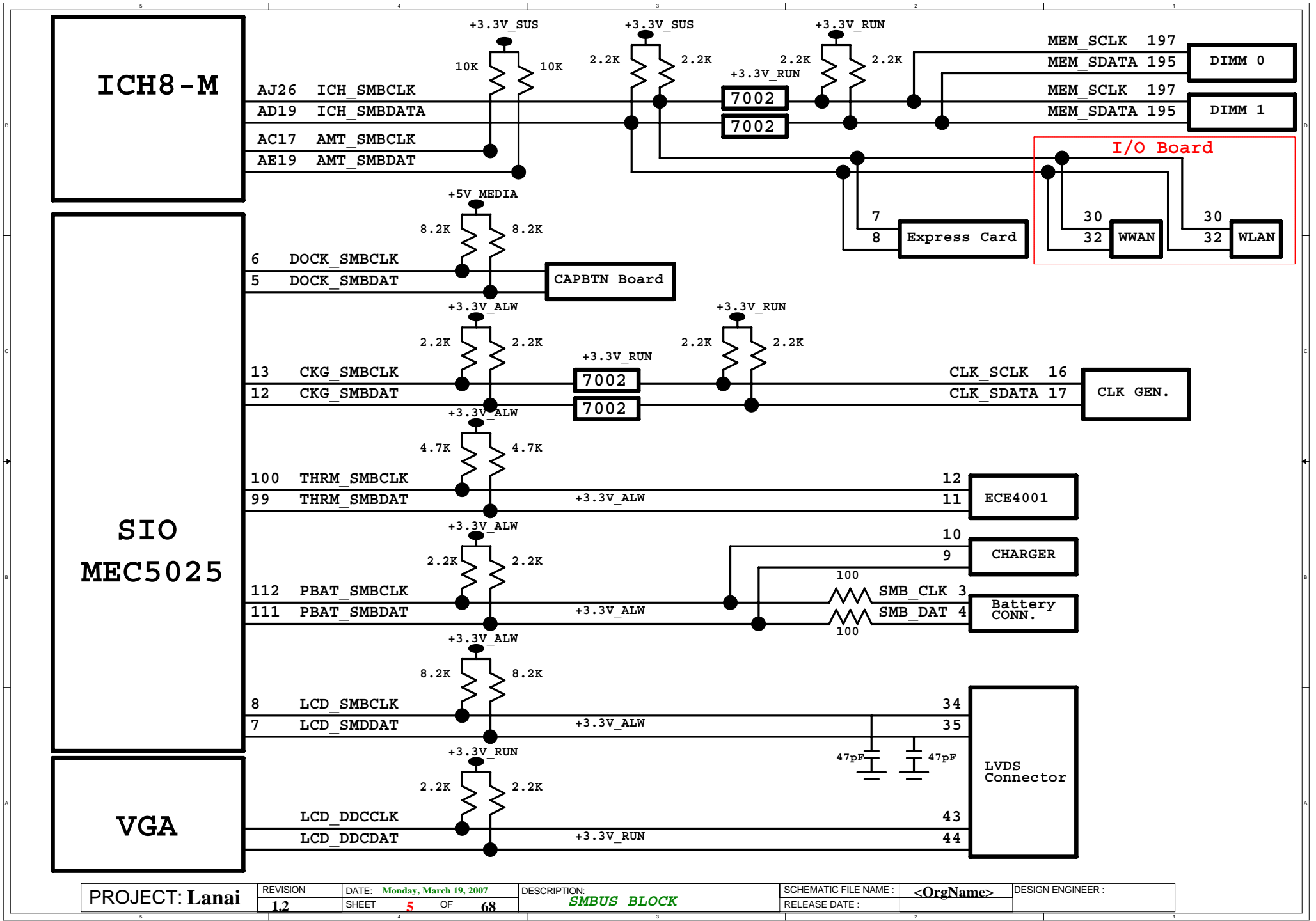
PCI TABLE			
PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

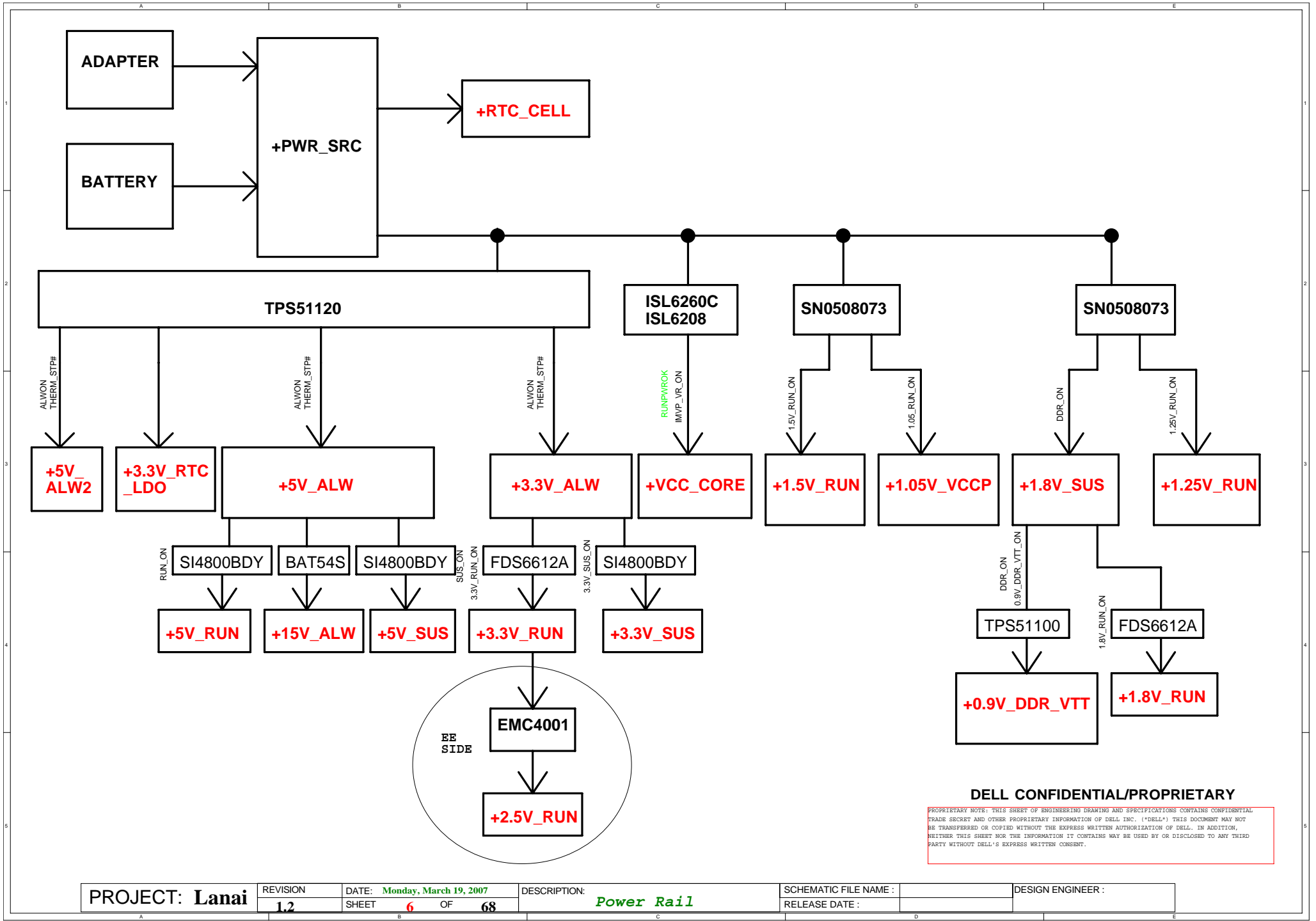
PCI Express TABLE	
Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

USB TABLE	
ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	User2 (Single port , in USB BD)
ICH8-2 (EHCI#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	
ICH8-5 (EHCI#1)	Camera
ICH8-6 (EHCI#2)	ExpressCard
ICH8-7 (EHCI#2)	BT Module
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	WWAN / Mini Card

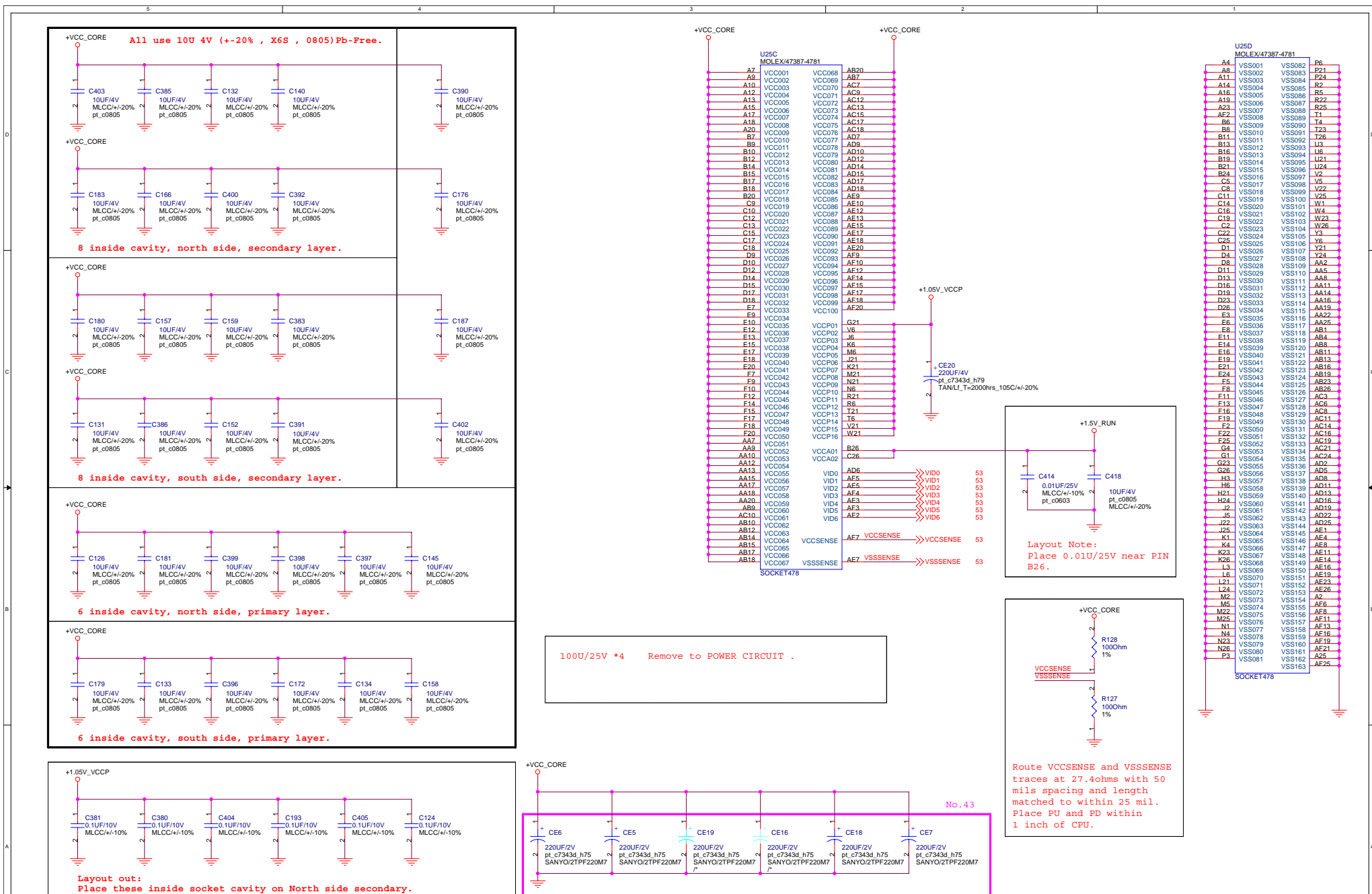
Note : No USB for WLAN

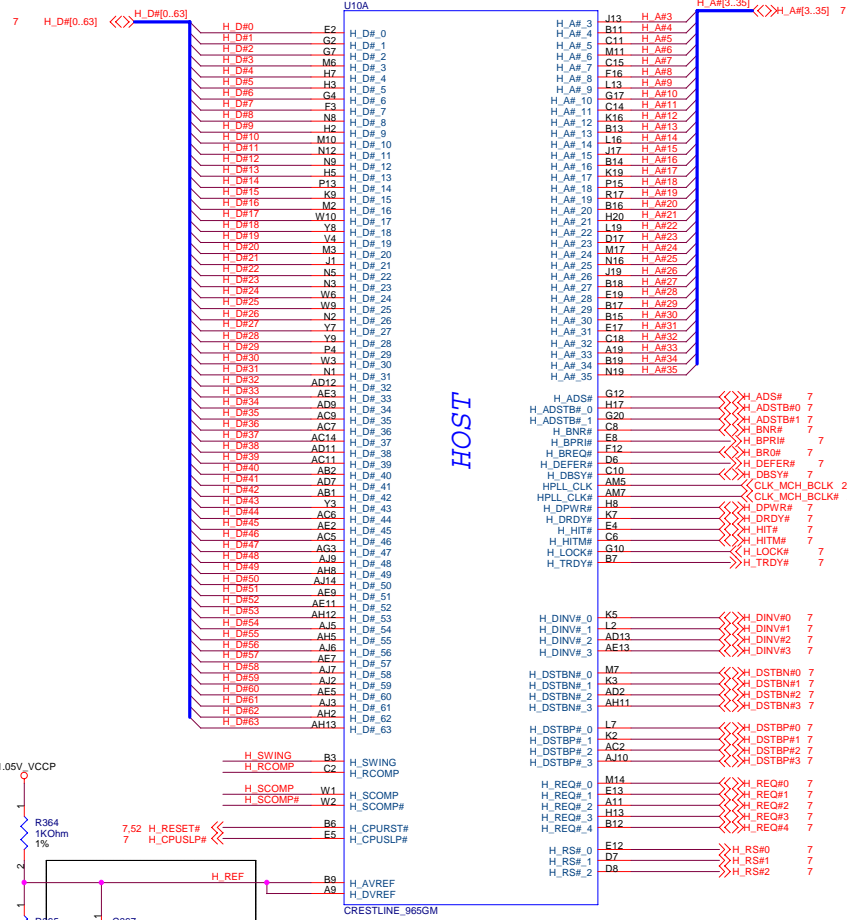
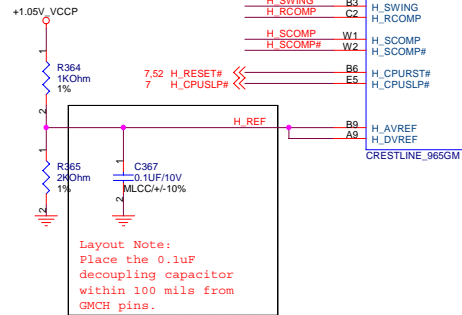
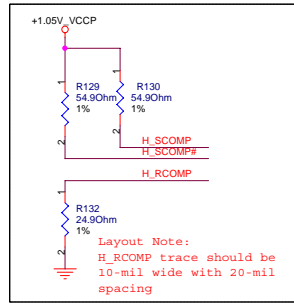
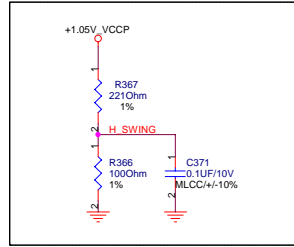
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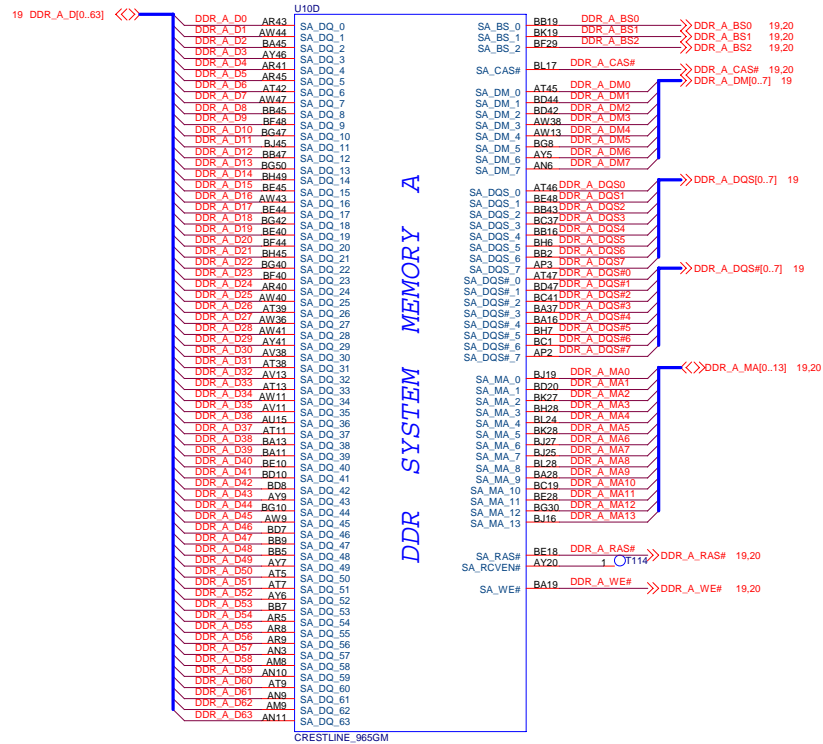






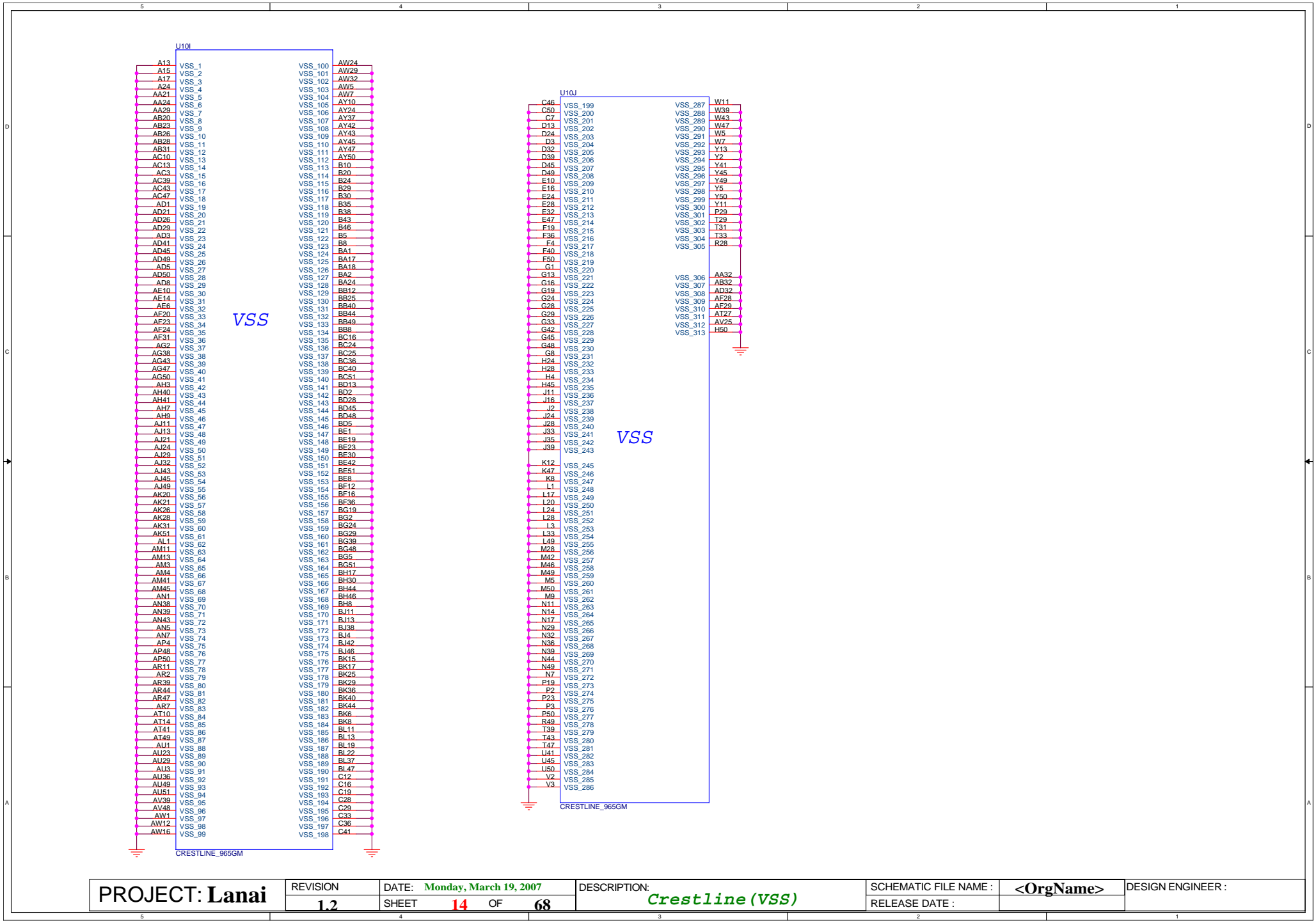
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: Crestline (HOST)	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
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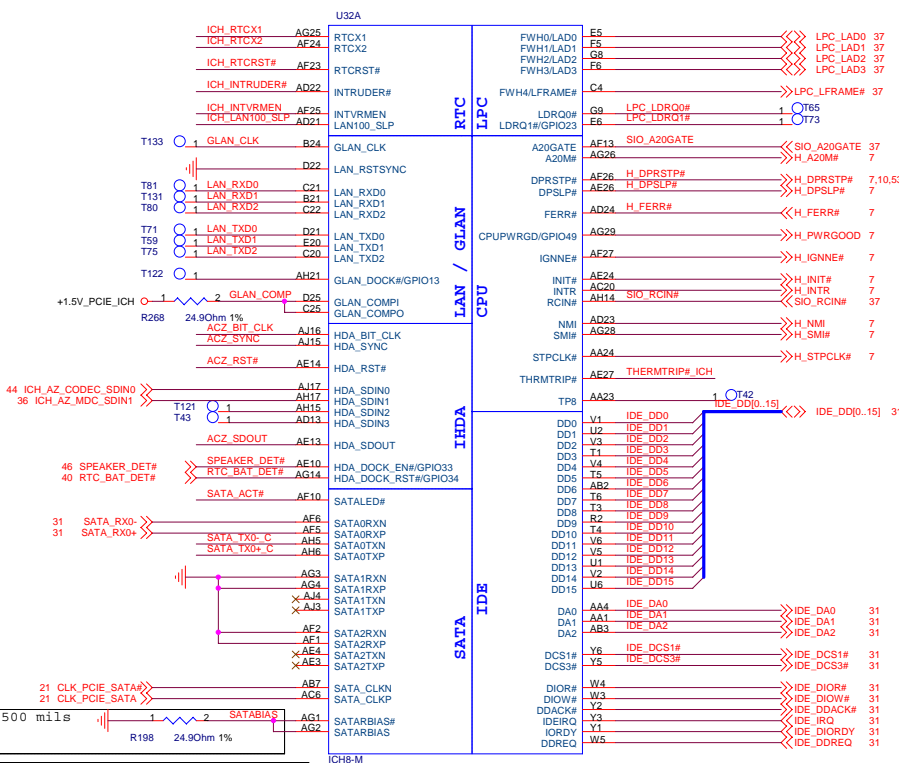
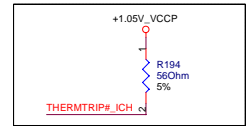
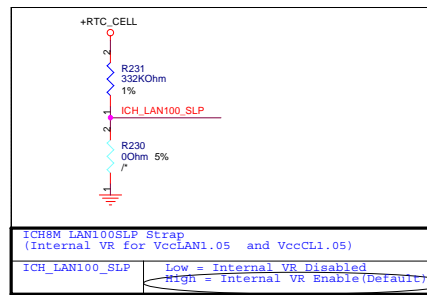
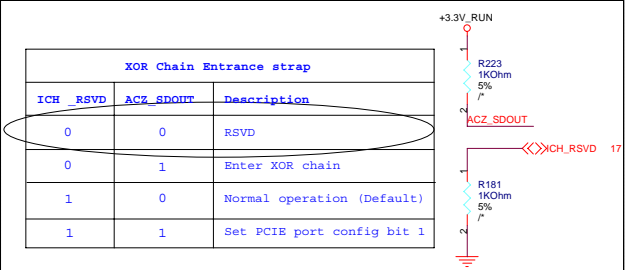
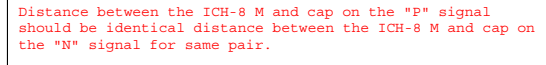
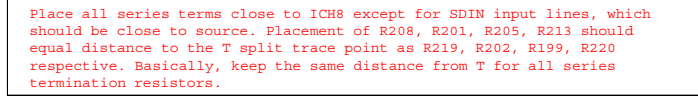
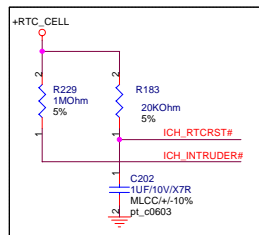




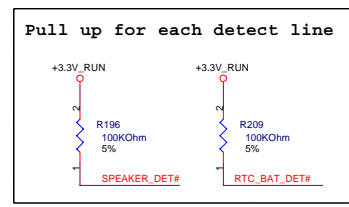
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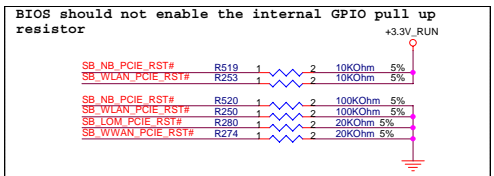
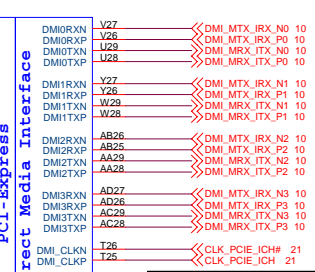
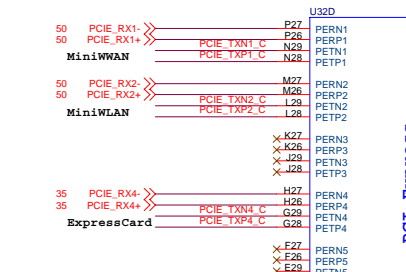
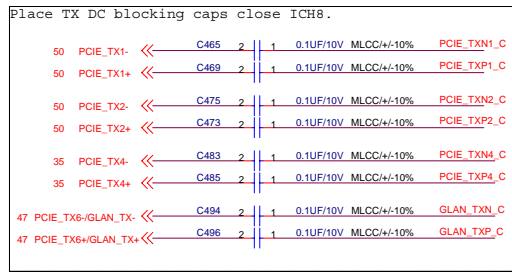




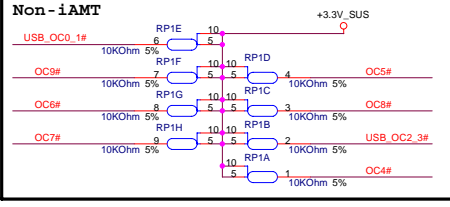
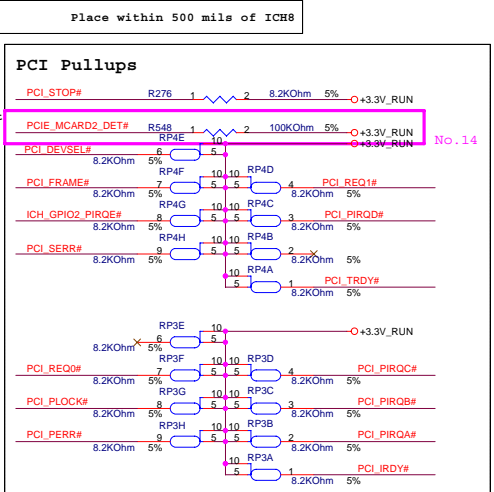
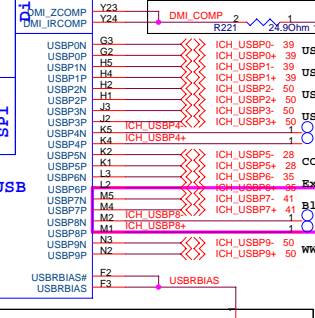
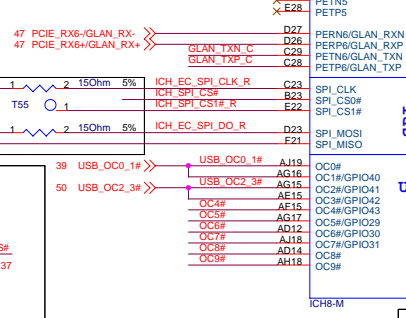
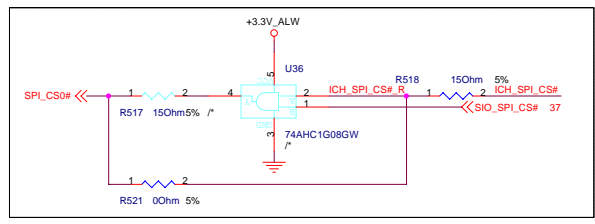


XOR Chain Entrance strap			
ICH	RSVD	ACQ_SDOIT	Description
0	0		RSVD
0	1		Enter XOR chain
1	0		Normal operation (Default)
1	1		Set PCIE port config bit 1

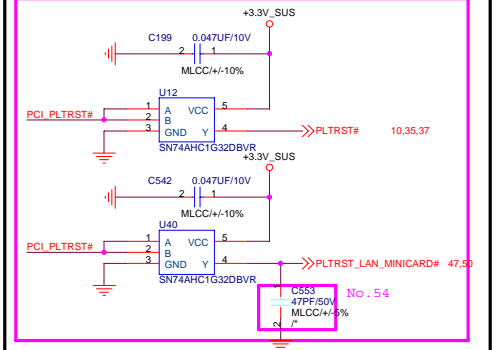
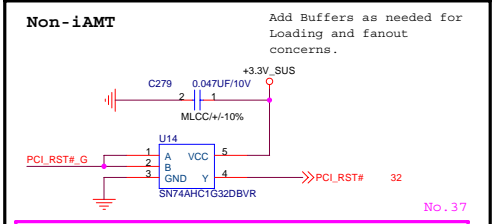
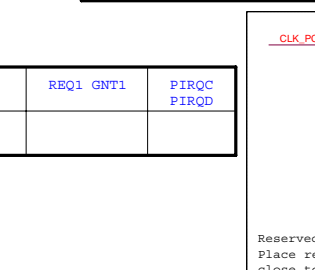
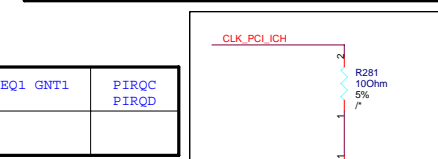
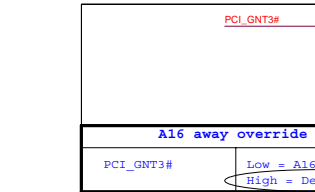
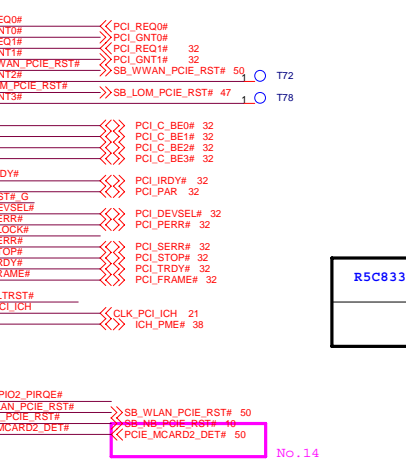
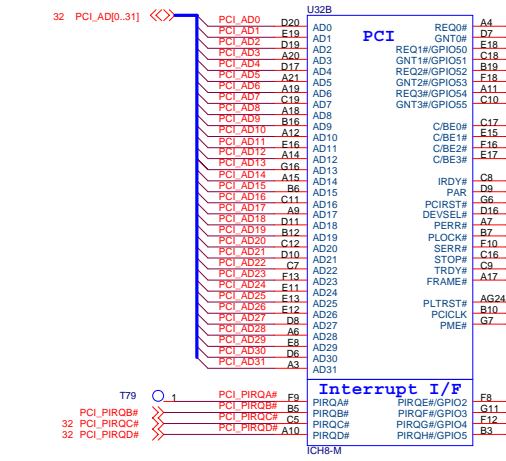
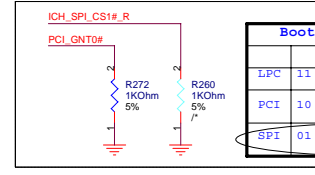




Layout Note:
Place 15 ohm within
500 mils from ICH.



Short F2 and F3 at the package
and keep length to less than
500mils. Trace Impedance
should be 60ohms +/- 15%.



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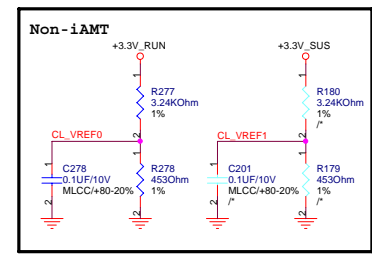
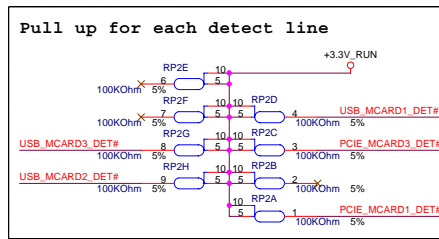
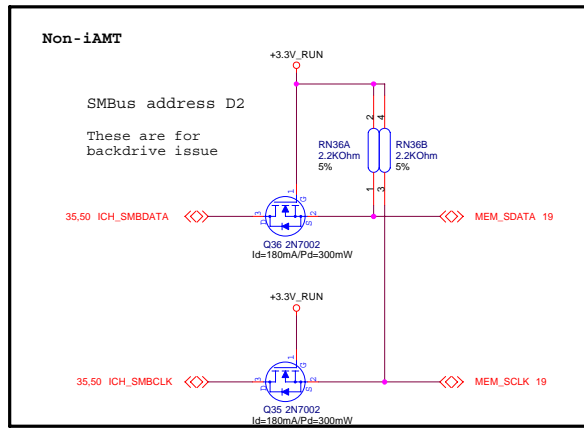
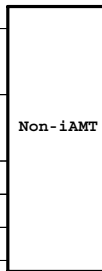
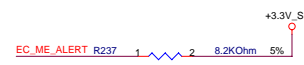
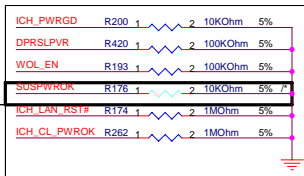
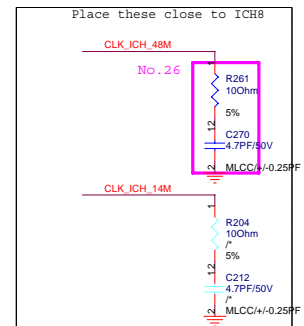
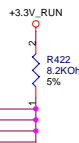
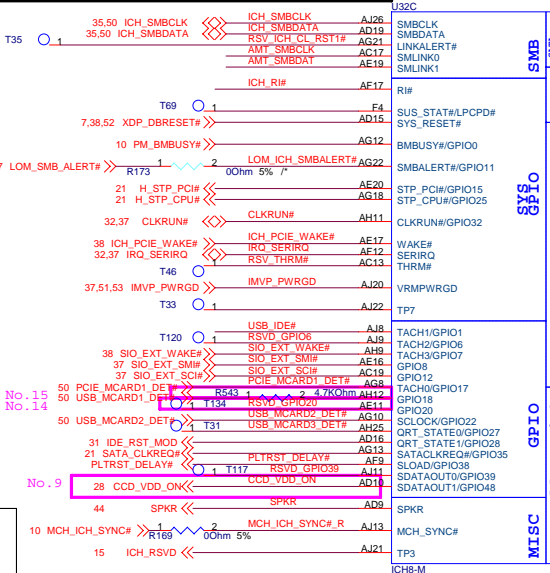
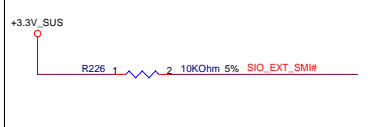
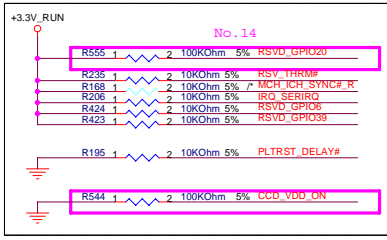
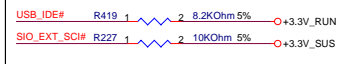
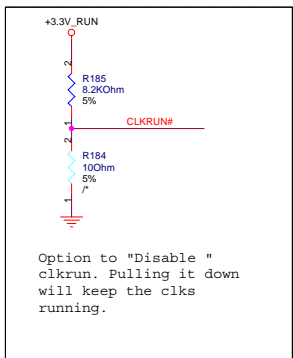
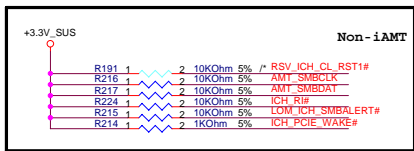
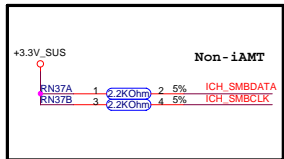
DESCRIPTION:
ICH8: PCI/INT/DMI/USB

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RELEASE DATE:

<OrgName>

DESIGN ENGINEER:

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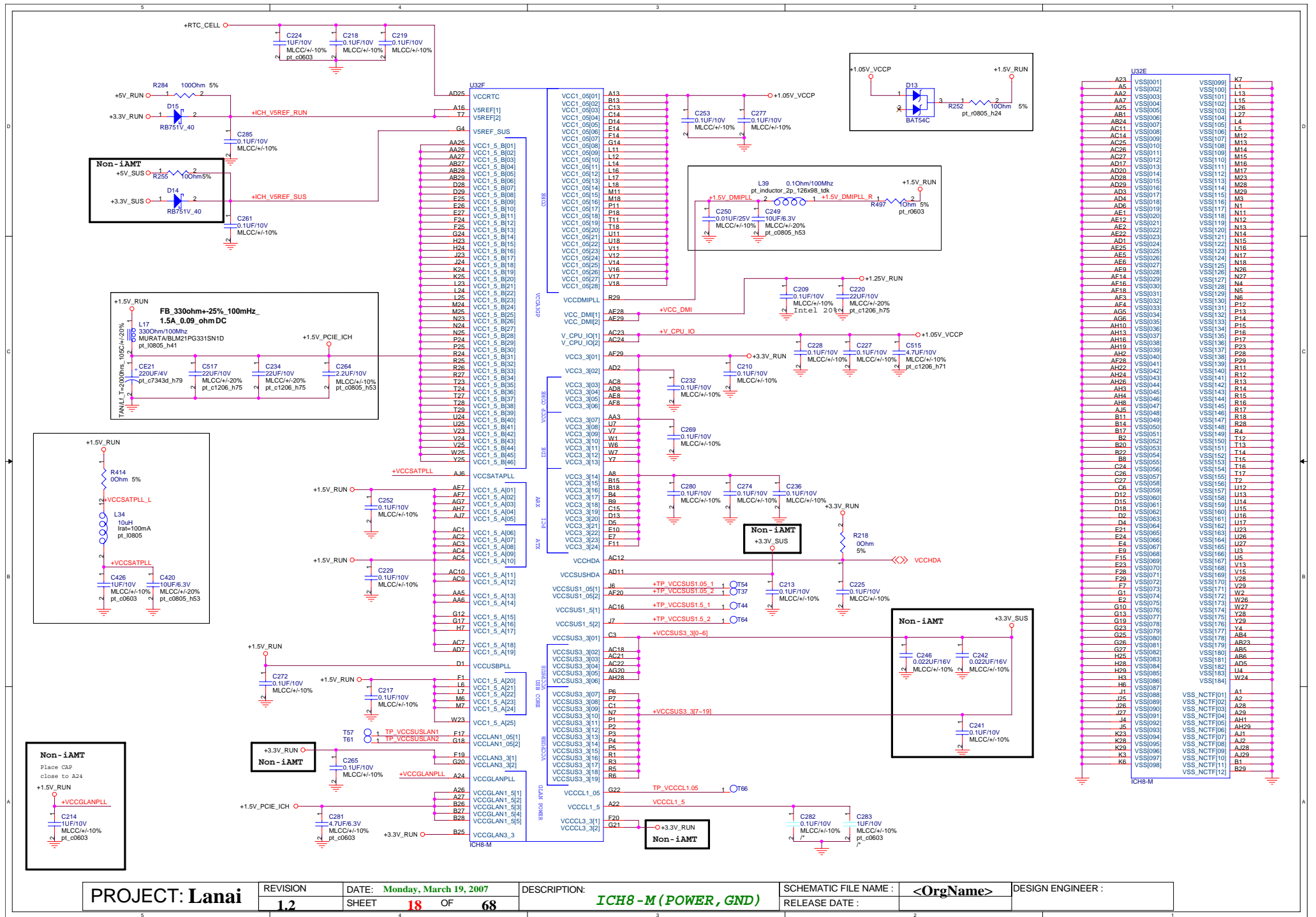
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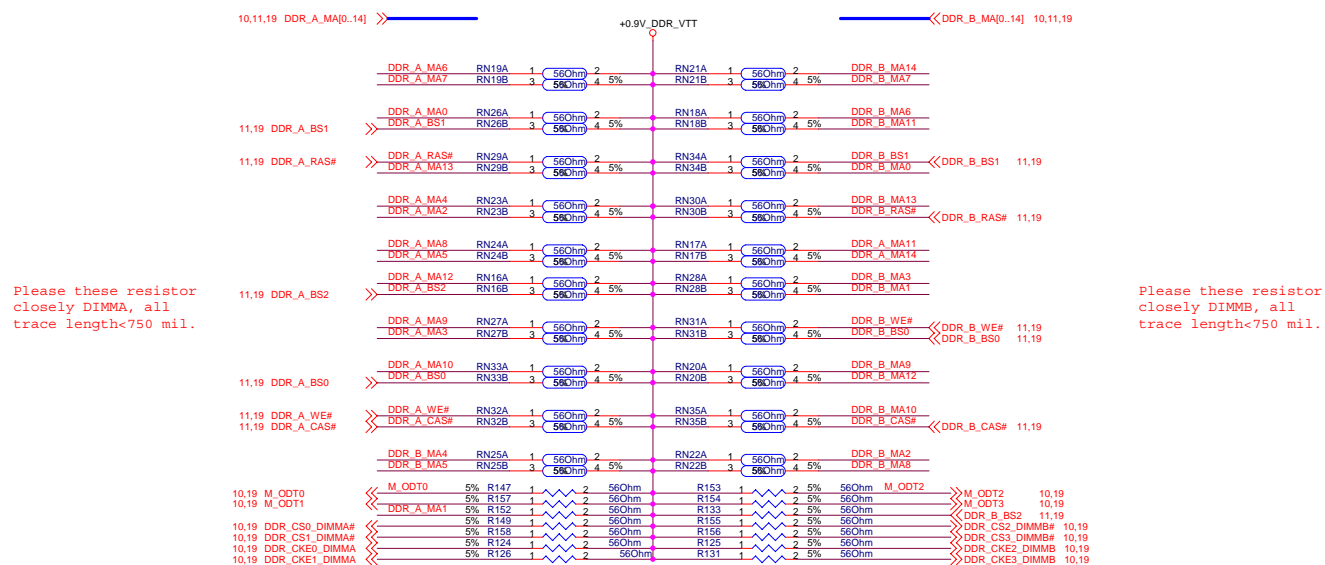
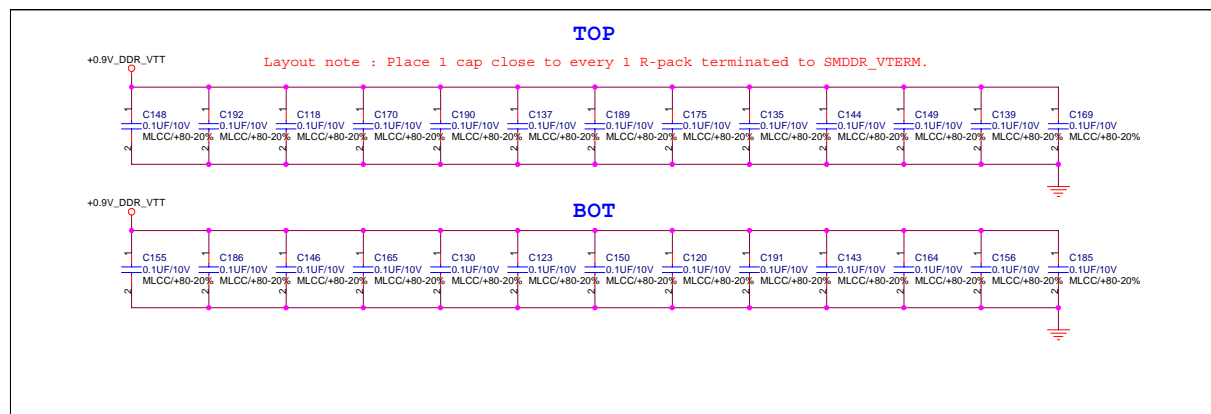
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DESCRIPTION:
ICH8: SMB/PWR/CLK/GPIO

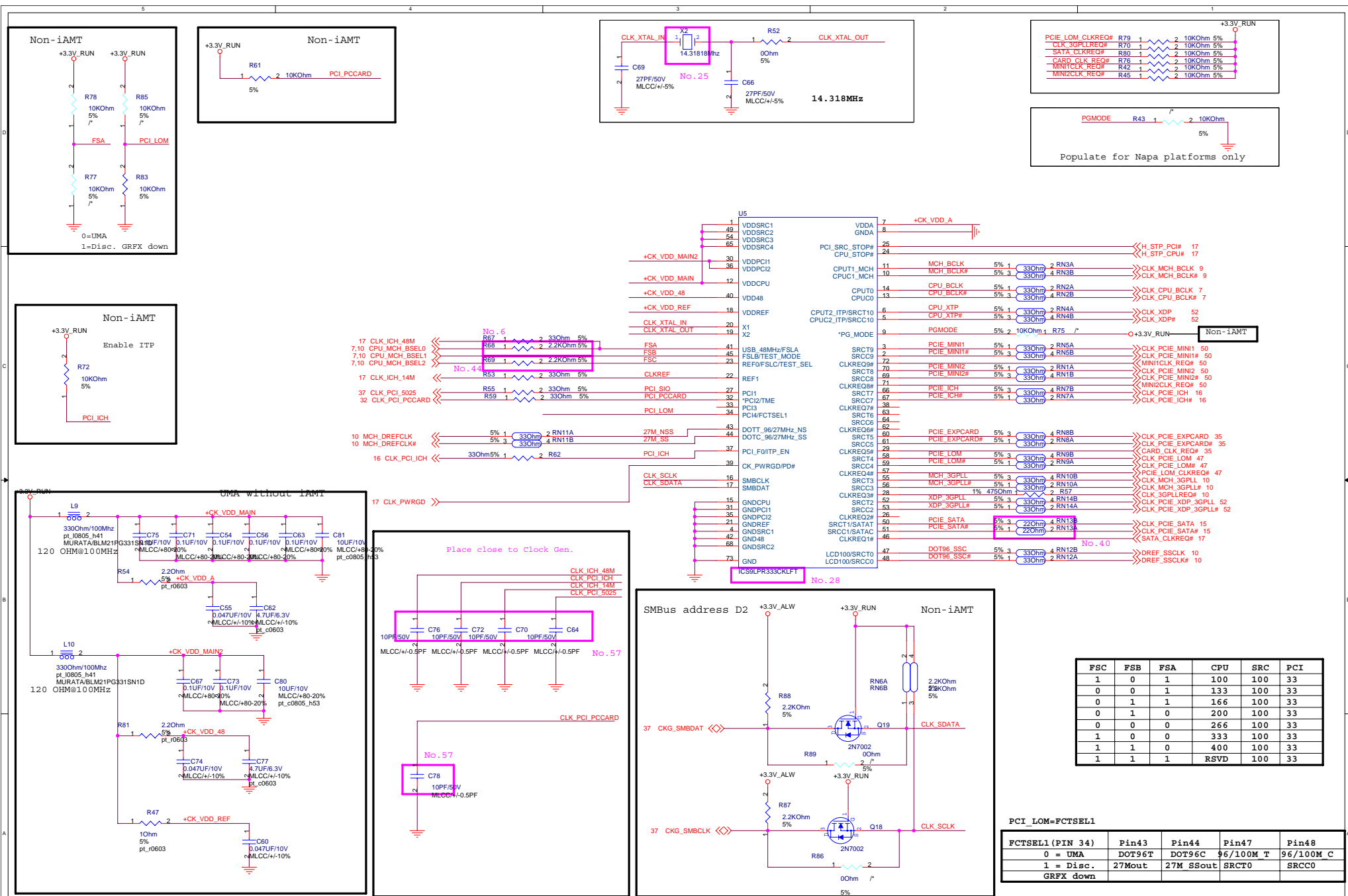
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RELEASE DATE:

DESIGN ENGINEER:





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DESCRIPTION: CLK GEN. CY28547

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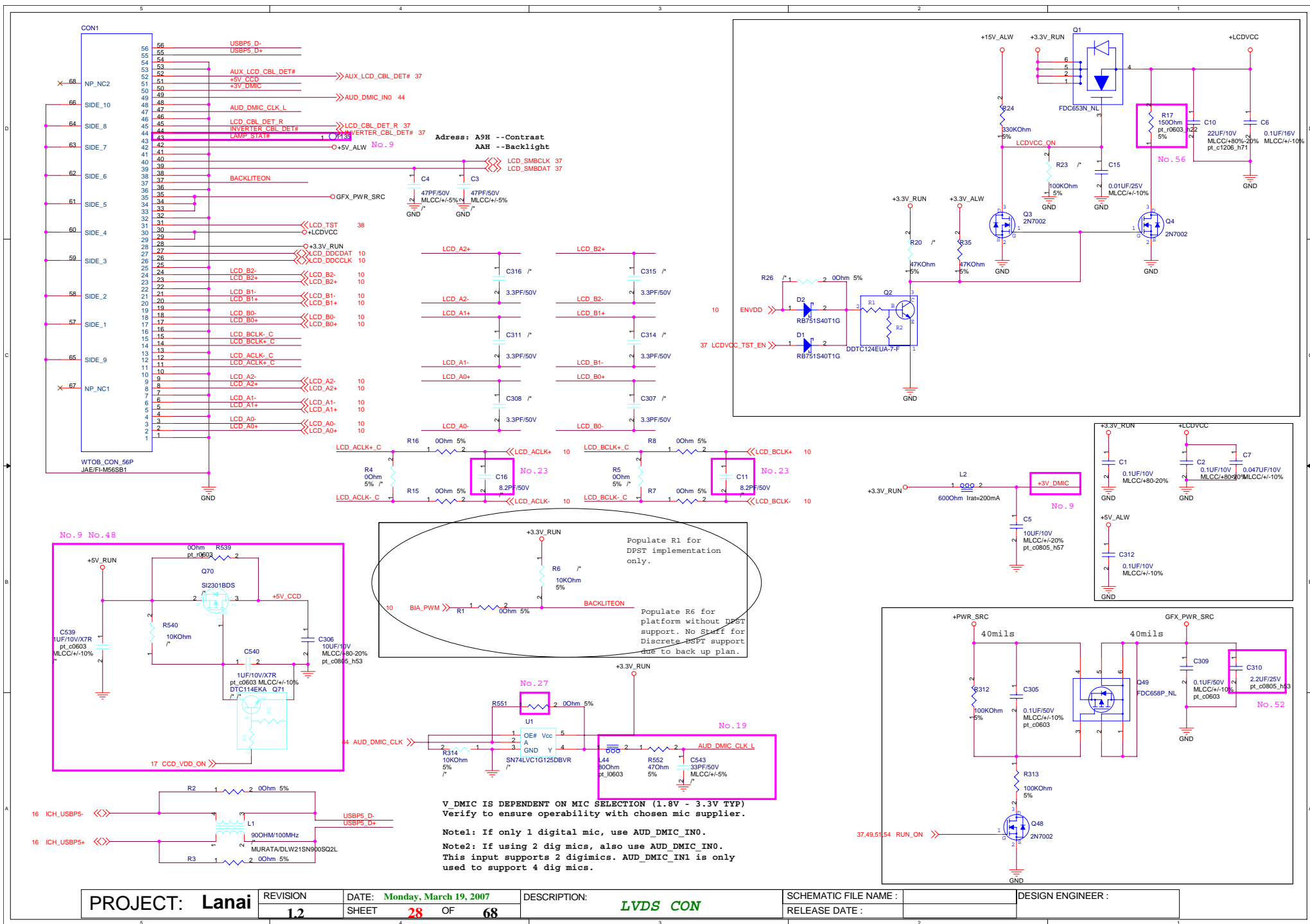
DESIGN ENGINEER:

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1									1
2									2
3									3
4									4
5									5
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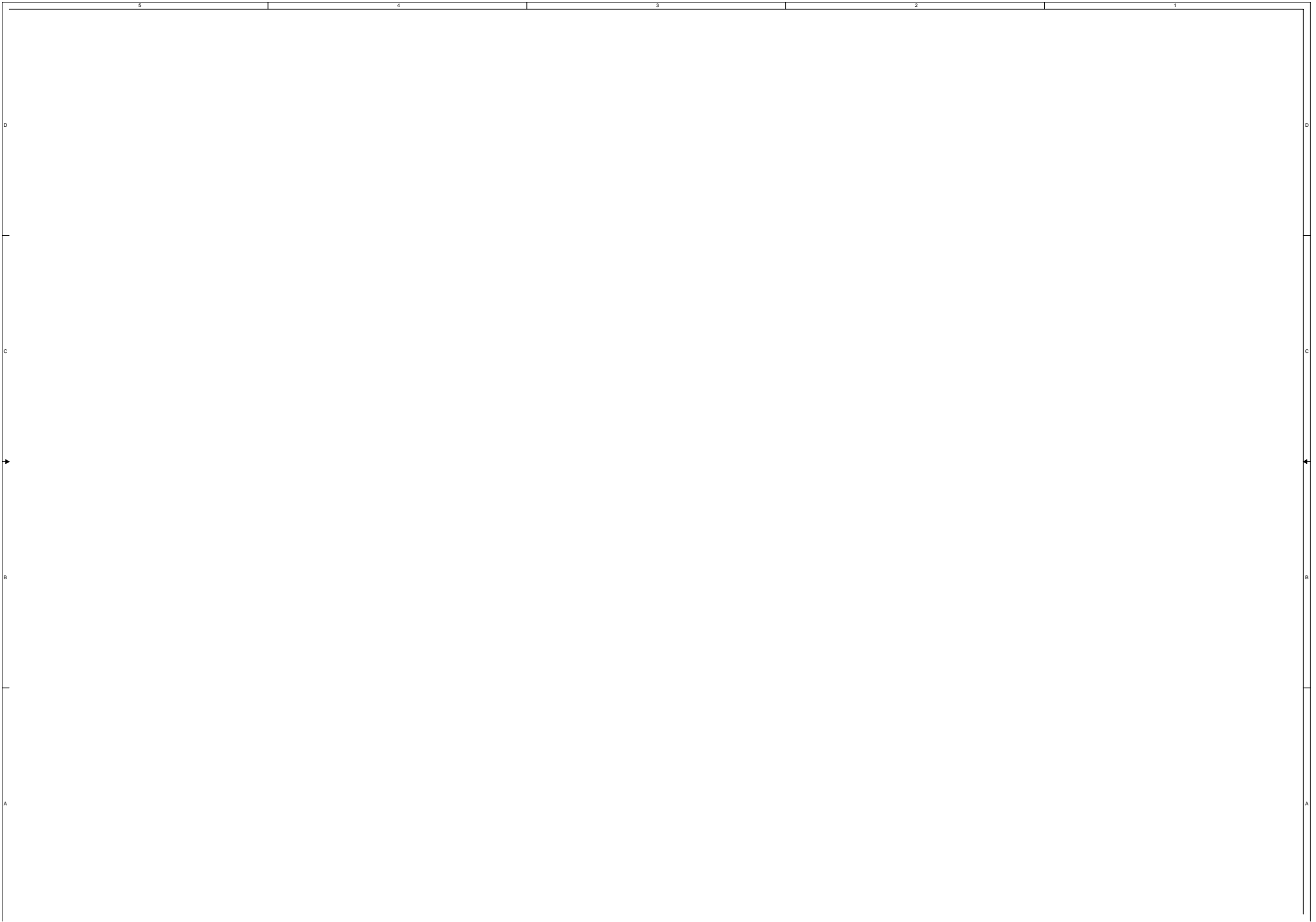
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DESCRIPTION: LVDS CON

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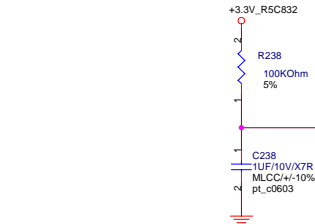
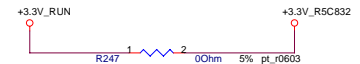
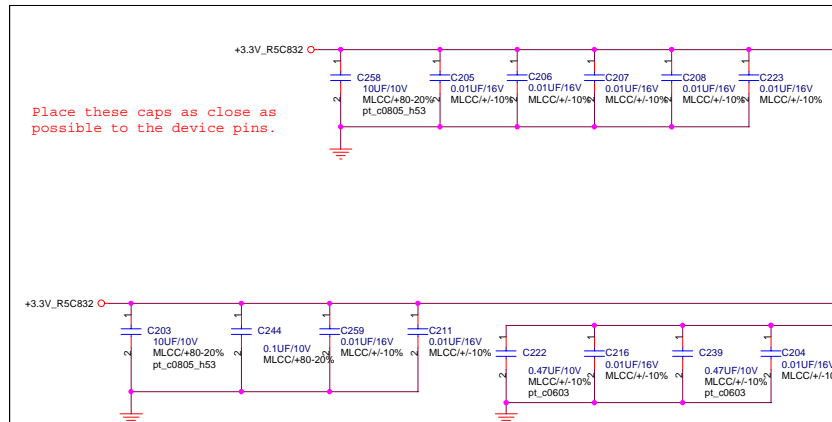
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ODD Connector

The schematic diagram illustrates the electrical connections for the ODD connector. It includes several power supply rails: +5V_MOD, +5V_ALW, +5V_ALW2, +5V_RUN, +5V_MOD, and +5V_RUN. The circuit features various components such as resistors (R254, R285, R270, R263, R244, R249, R241, R248, R256), capacitors (C254, C268, C281, C240, C267, C287), and integrated circuits (ICs) like the SI4800BDY MOSFET (Q41), the 2N7002 NMOS transistor (Q43, Q44), and the SUYIN/800194MR050S520ZL IC. The diagram also shows the connection of the IDE_00[0:15] bus to the IDE_DD[0:15] bus and the IDE_DREQ signal to the IDE_DREQ pin. A note indicates that the capacitors should be placed close to the connectors.

Place caps close to connector.

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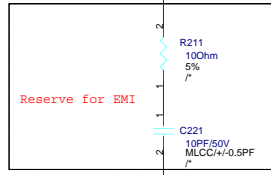


16 PCI_AD[0..31]

16 PCI_PAR
16 PCI_C_BE3#
16 PCI_C_BE2#
16 PCI_C_BE1#
16 PCI_C_BE0#

16 PCI_AD17 >> PCI_AD17
16 PCI_REQ1#
16 PCI_GNT1#
16 PCI_FRAME#
16 PCI_IRDY#
16 PCI_TRDY#
16 PCI_DEVSEL#
16 PCI_STOP#
16 PCI_PERR#
16 PCI_SERR#

Route to CLK_GEN .
21 CLK_PCI_PCCARD >>



Pull-up to +3.3V_ALW is required on SYS_PME# on SIO schematics. (From SIO). 0 ohm of PME# is no-stuff to prevent backdrive from this signal since the controller is powered of the RUN rail

17.37 CLKRUN# >> R222 1 00hm 5%
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive the signal low, in order to disable CLKRUN#.

U31B
10 VCC_PCI3V_1
20 VCC_PCI3V_2
27 VCC_PCI3V_3
32 VCC_PCI3V_4
41 VCC_PCI3V_5
128 VCC_PCI3V_6
61 VCC_RIN
16 VCC_OUT1
34 VCC_OUT2
64 VCC_OUT3
114 VCC_OUT4
120 VCC_OUT5

16 VCC_MD
67 VCC_3V
61 VCC_RIN
16 VCC_OUT1
34 VCC_OUT2
64 VCC_OUT3
114 VCC_OUT4
120 VCC_OUT5

125 AD31
126 AD30
127 AD29
1 AD28
2 AD27
3 AD26
5 AD25
6 AD24
9 AD23
11 AD22
12 AD21
14 AD20
15 AD19
17 AD18
18 AD17
19 AD16
36 AD15
37 AD14
38 AD13
39 AD12
40 AD11
42 AD10
43 AD9
44 AD8
46 AD7
47 AD6
48 AD5
49 AD4
50 AD3
51 AD2
52 AD1
53 AD0

16 PCI_PAR
16 PCI_C_BE3#
16 PCI_C_BE2#
16 PCI_C_BE1#
16 PCI_C_BE0#

16 PCI_AD17 >> PCI_AD17
16 PCI_REQ1#
16 PCI_GNT1#
16 PCI_FRAME#
16 PCI_IRDY#
16 PCI_TRDY#
16 PCI_DEVSEL#
16 PCI_STOP#
16 PCI_PERR#
16 PCI_SERR#

16 PCI_RST# >>
16 SYS_PME# >> R486 1 00hm 5%
17.37 CLKRUN# >> R222 1 00hm 5%
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive the signal low, in order to disable CLKRUN#.

124 REQ#
123 GNT#
23 FRAME#
24 IRDY#
25 TRDY#
26 DEVSEL#
29 STOP#
30 PERR#
31 SERR#

71 GBRST#
119 PCIRST#
121 PCICLK
70 PME#
117 CLKRUN#

R5C833 TQFP128
C.S R5C833 TQFP128
No.24

Ricoh R5C832 Package Type : TQFP-128-P1 (1414)

4 GND1
13 GND2
22 GND3
28 GND4
54 GND5
62 GND6
63 GND7
68 GND8
118 GND9
122 GND10
99 AGND1
102 AGND3
103 AGND2
107 AGND4
111 AGND5

69 HWSPND#
58 MSEN
55 XDEN
57 UIDIO5
65 UIDIO3
59 UIDIO4
56 UIDIO2
60 UIDIO1
72 UIDIO/SRIRQ#

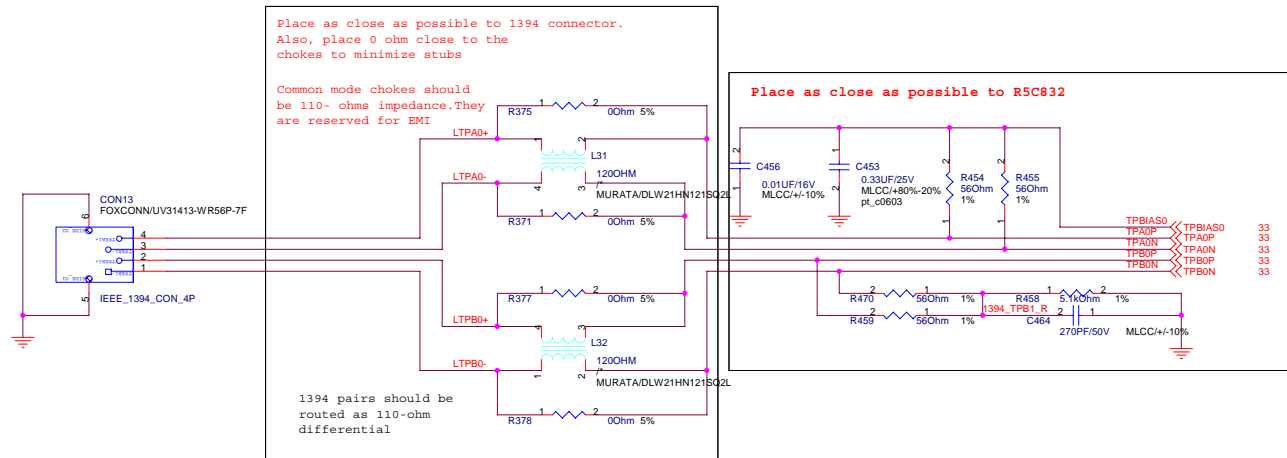
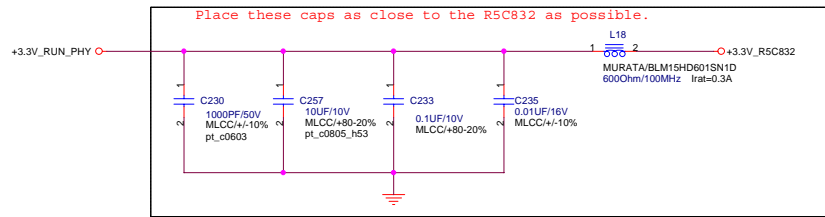
1 R239 10KOhm 5% +3.3V_R5C832 Memory Stick Enable
2 R236 100KOhm 5% +3.3V_R5C832 XD Card Enable
1 R239 10KOhm 5% +3.3V_R5C832 Serial ROM disable
2 R236 100KOhm 5% +3.3V_R5C832 SD Card Enable
1 R239 10KOhm 5% +3.3V_R5C832 MMC Card Enable

115 INTA# >> PCI_PIRQD# 16 1394 : INTA#
116 INTB# >> PCI_PIRQC# 16 4in1 : INTB#

115 INTA# >> PCI_PIRQD# 16 1394 : INTA#
116 INTB# >> PCI_PIRQC# 16 4in1 : INTB#

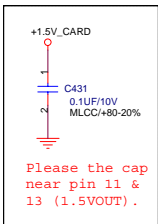
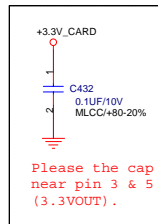
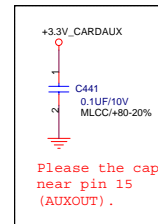
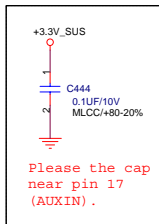
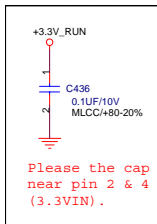
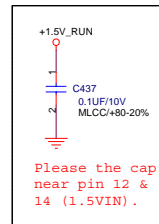
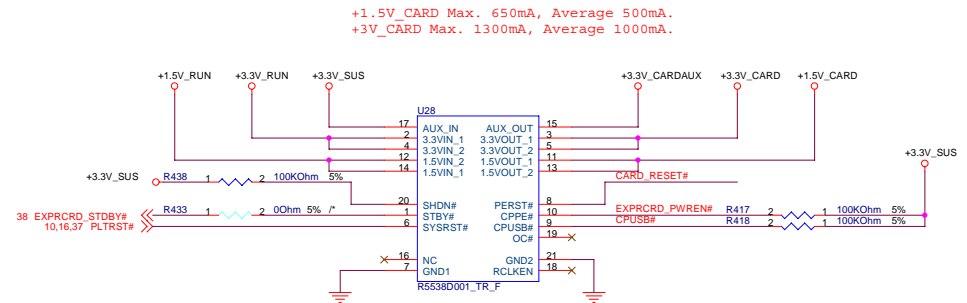
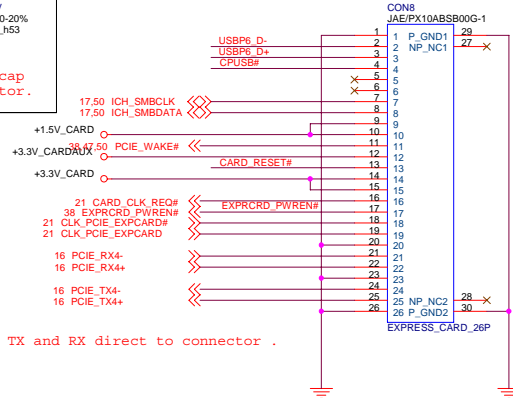
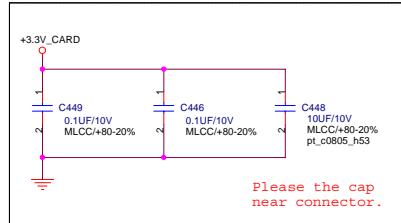
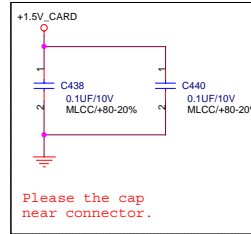
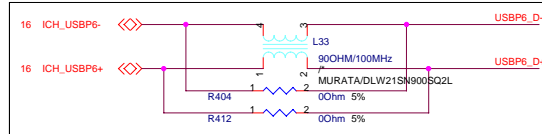
66 TEST
1 T129
R487 100KOhm 5%

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: R5C833 - PCI INTERFACE	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER :
		SHEET 32 OF 68		RELEASE DATE :	

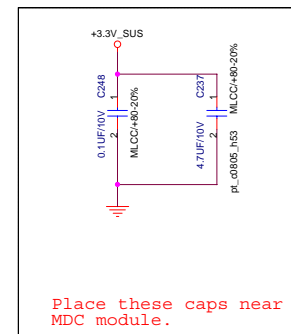
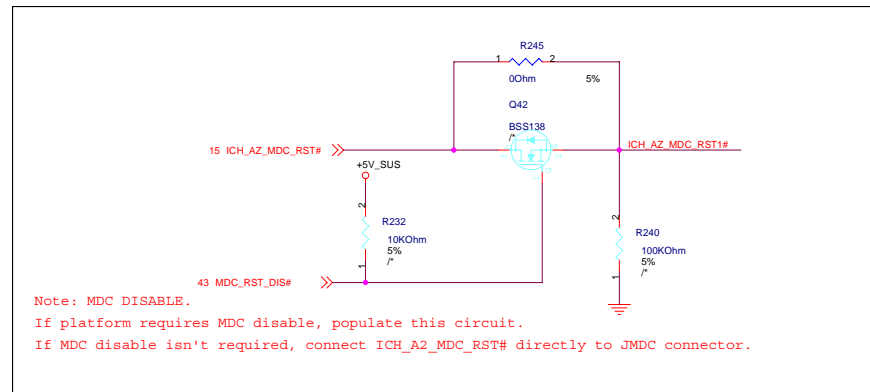
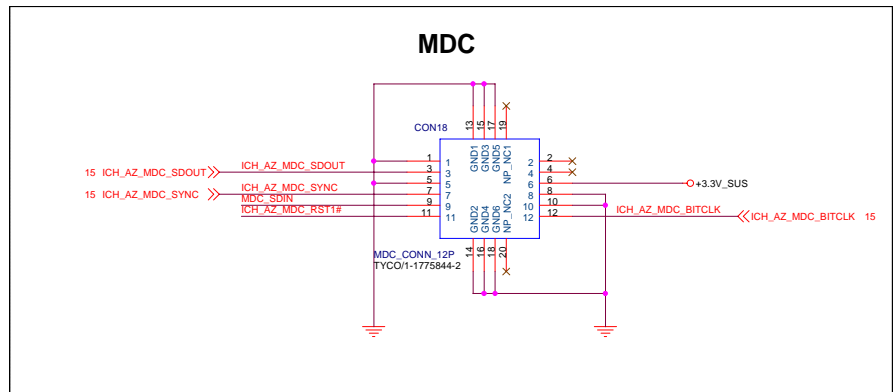


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: R5C833 - IEEE1394 PART	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 34 OF 68		RELEASE DATE :		

Express Card

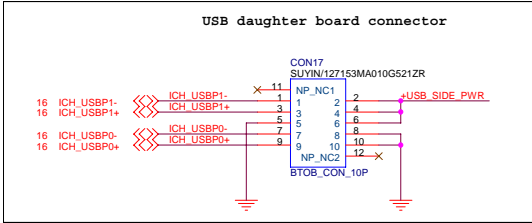
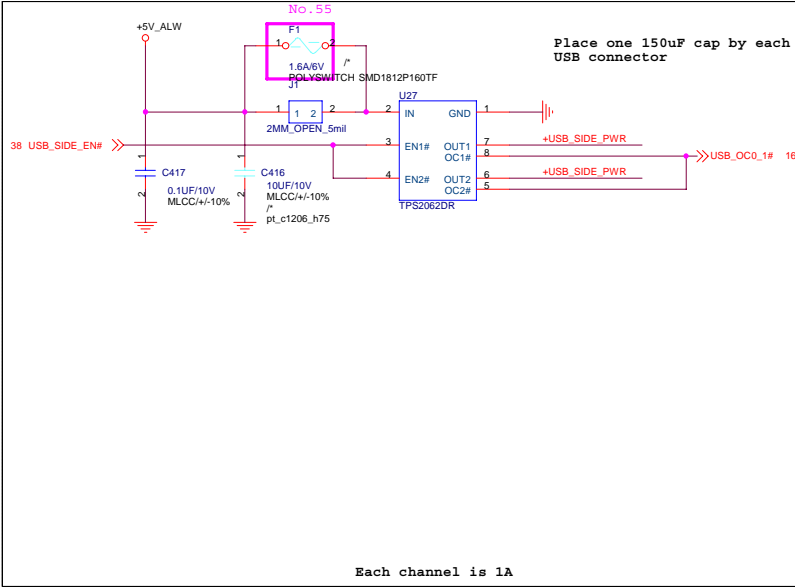


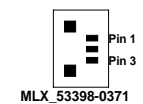
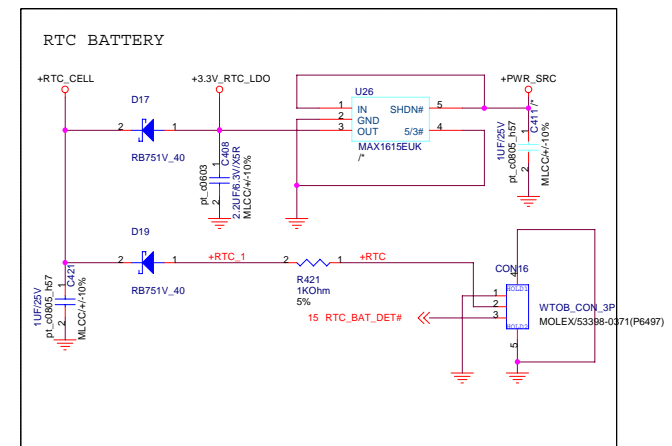
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: PCI-Express Card	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: Terry Lin
	1.2	SHEET 35 OF 68			



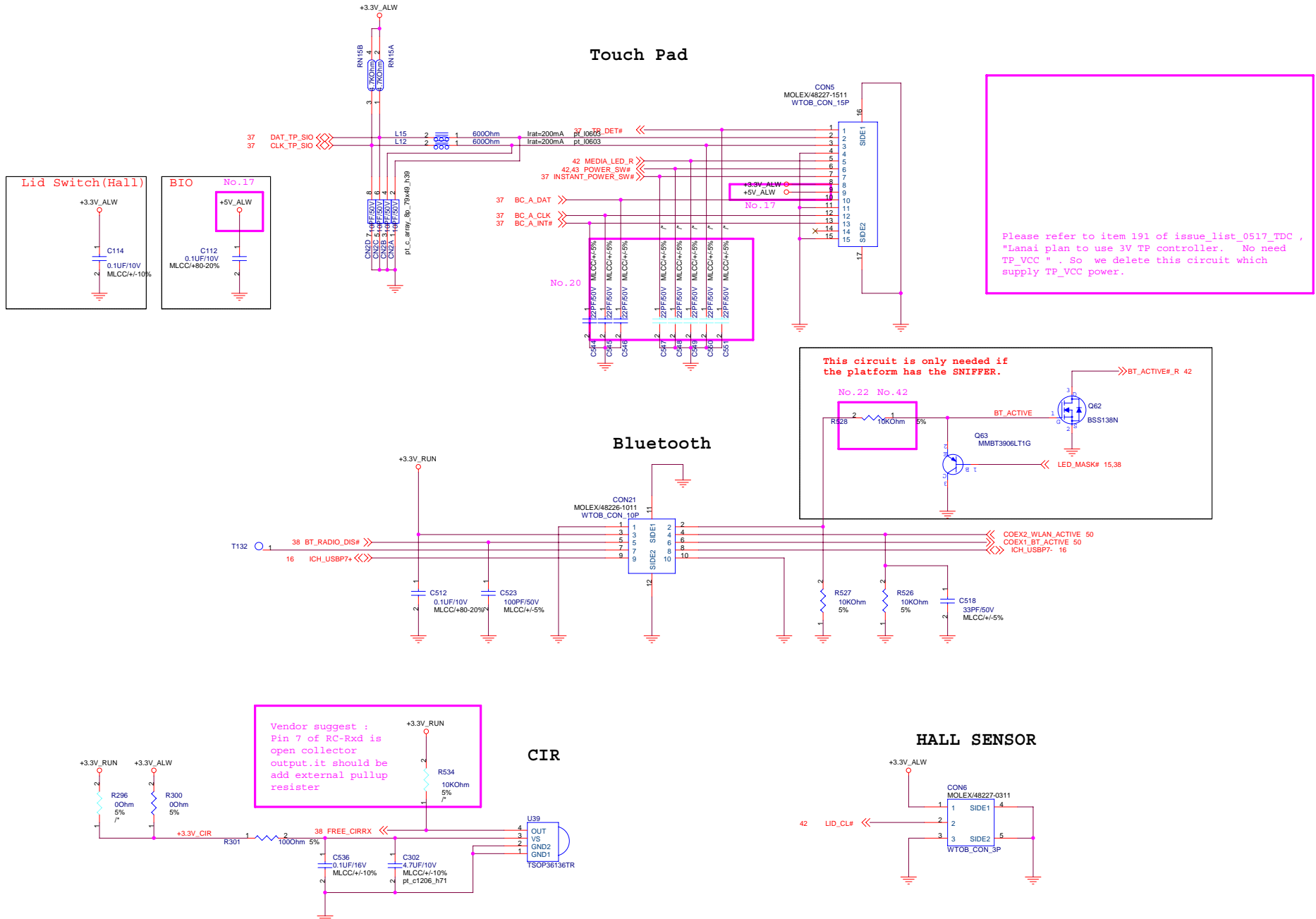
文才专用——



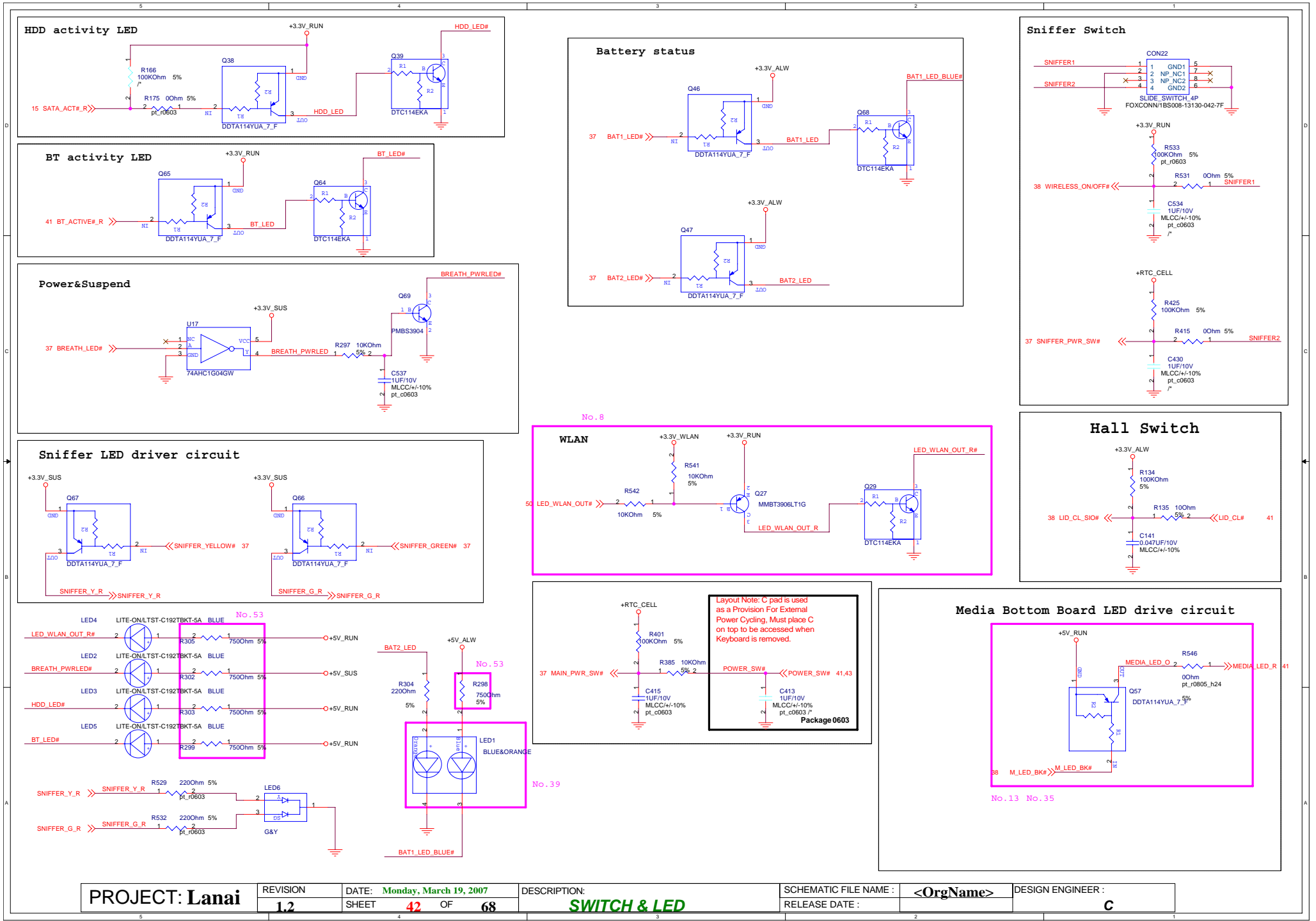


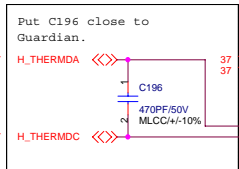
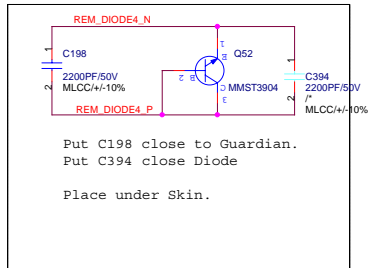
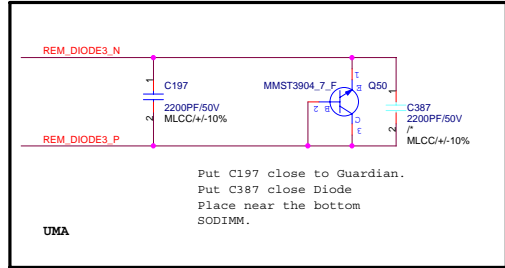
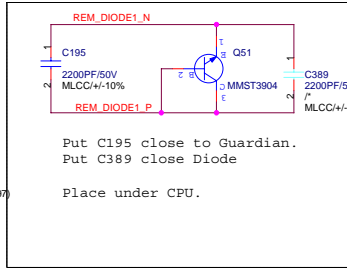
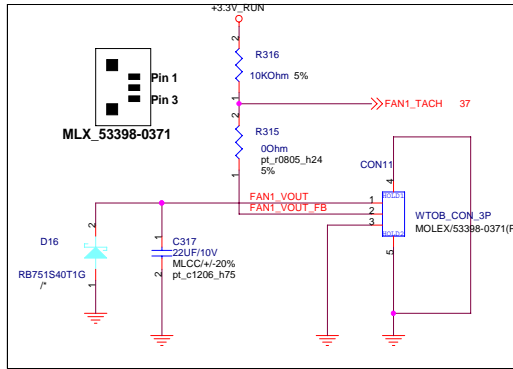


PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: FLASH & RTC	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : C.L. Ho
	1.2	SHEET 40 OF 68		RELEASE DATE :		



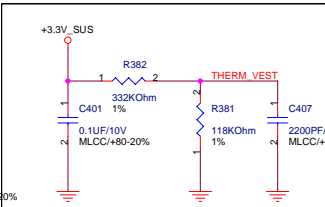
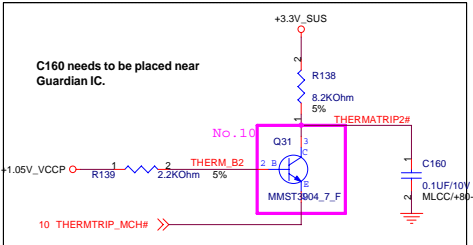
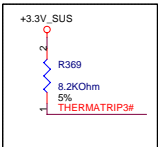
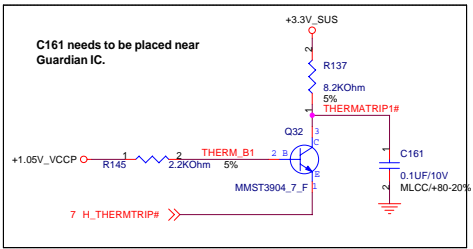
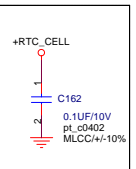
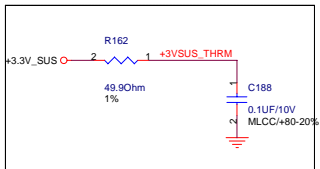
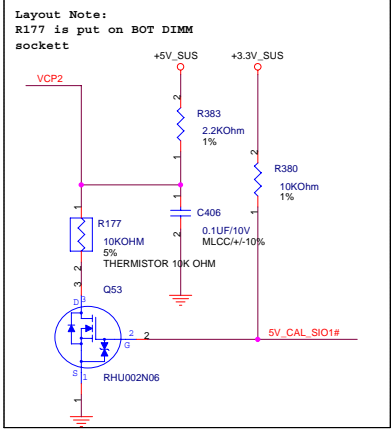
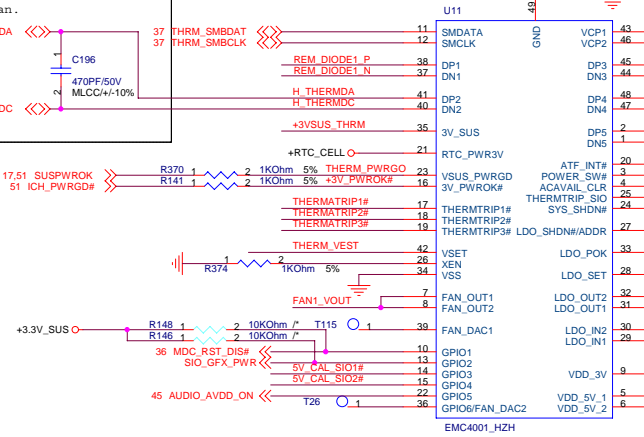
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: TOUCH PAD & BT & CIR & LID	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
	1.2	SHEET 41 OF 68			



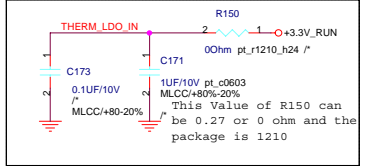
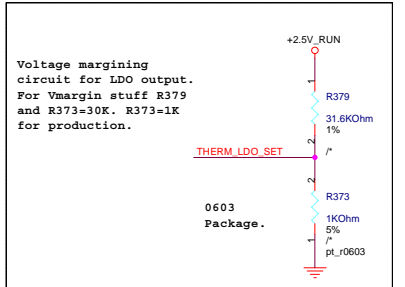
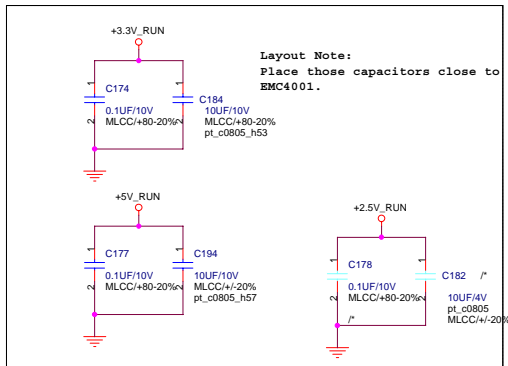


Guardian

Note:
150K input impedance on VCP1 (Pin 43)



Note:
VSET = (Tp-70)/21, where Tp = 70 to 101 degree C.
Tp set at 88 degrees C.
Guardian temp tolerance = +/- 3 degrees C.



PROJECT: Lanai

REVISION 1.2

DATE: Monday, March 19, 2007
SHEET 43 OF 68

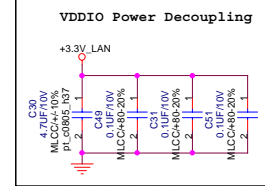
DESCRIPTION: EMC4001

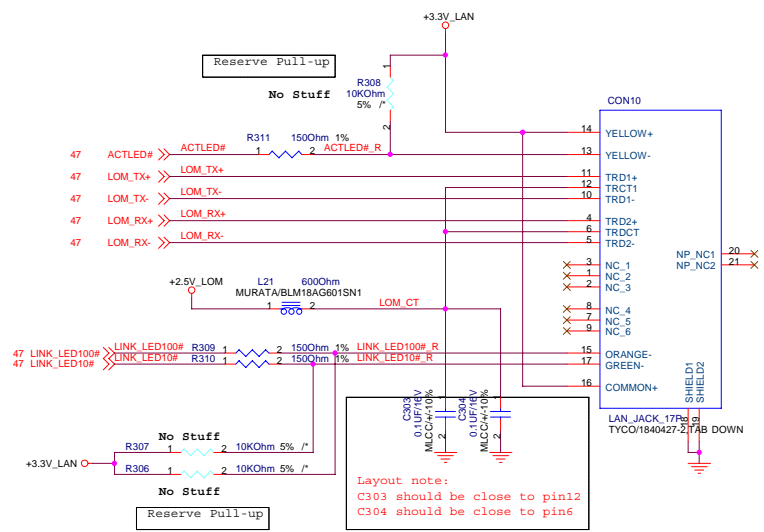
SCHEMATIC FILE NAME :

RELEASE DATE :

DESIGN ENGINEER :

N

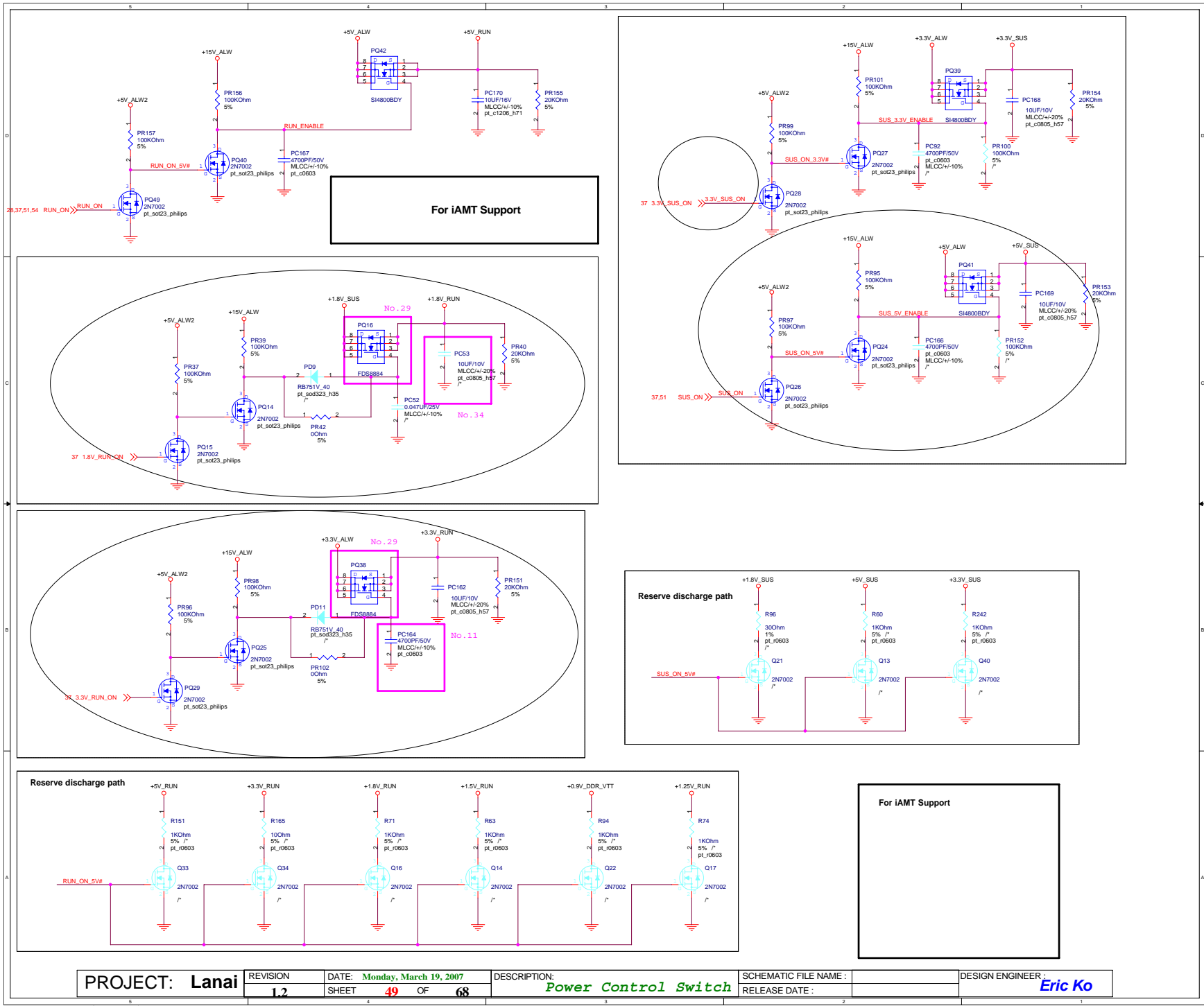




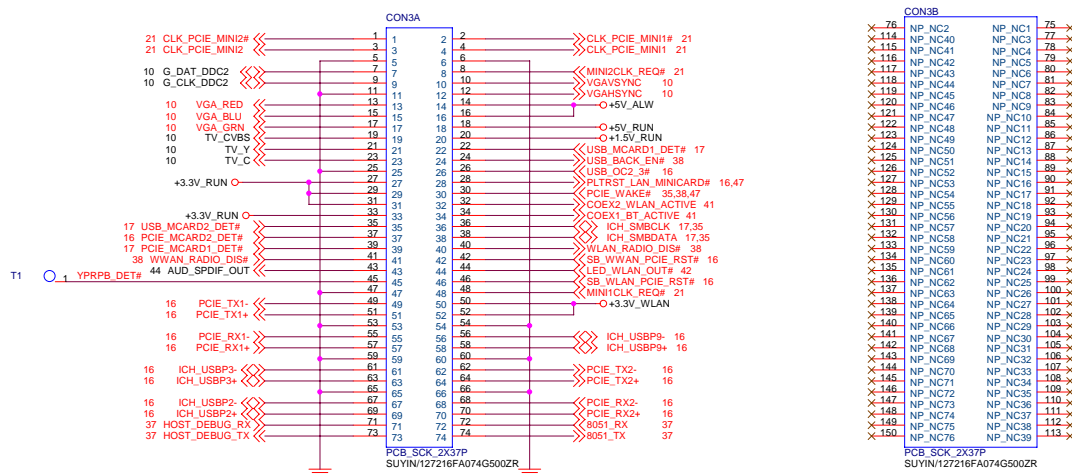
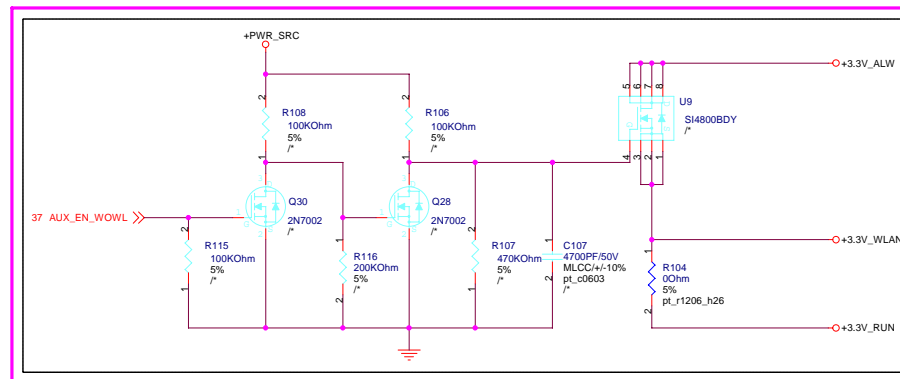
+3.3V LAN Source Guideline:

1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on-LAN is required out of S4, S5

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: Magnetics and RJ-45	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Ivan Chou
	1.2	SHEET 48 OF 68			



No. 21



PROJECT: Lanai

REVISION
1.2

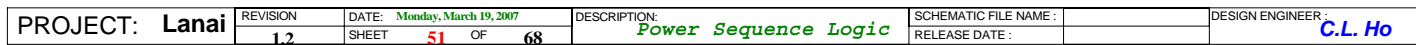
DATE: Monday, March 19, 2007
SHEET 50 OF 68

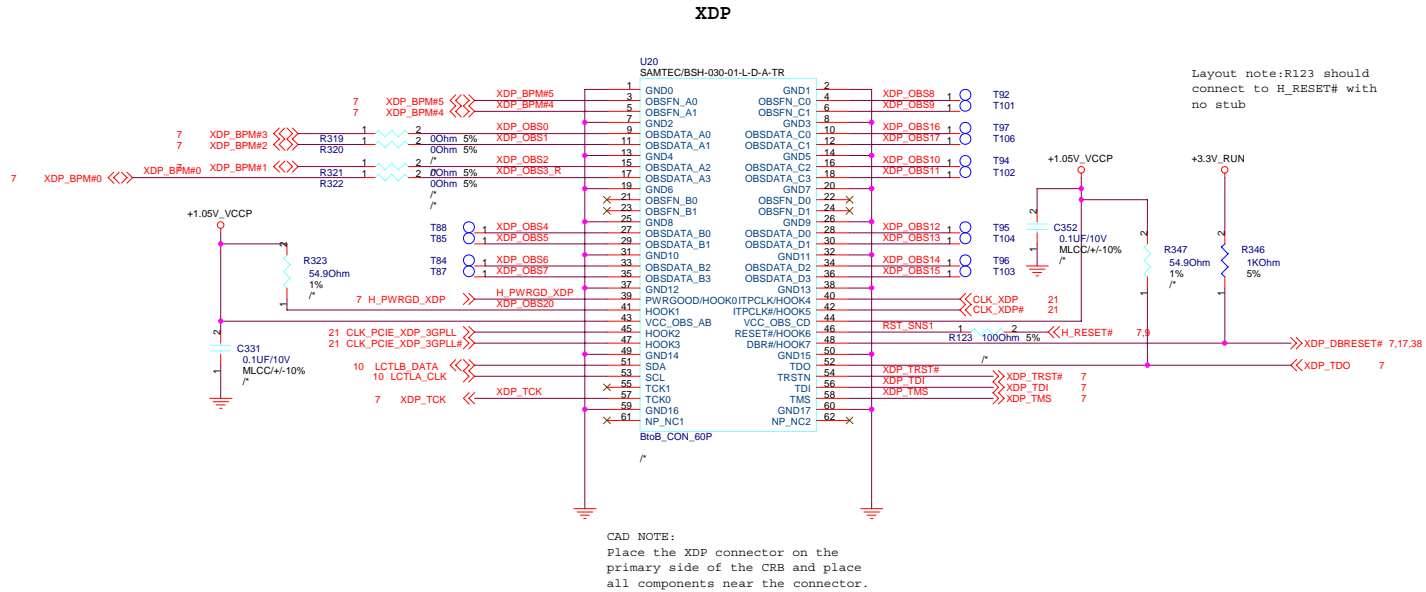
DESCRIPTION: BtoB CON

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER :
STANLY HSU

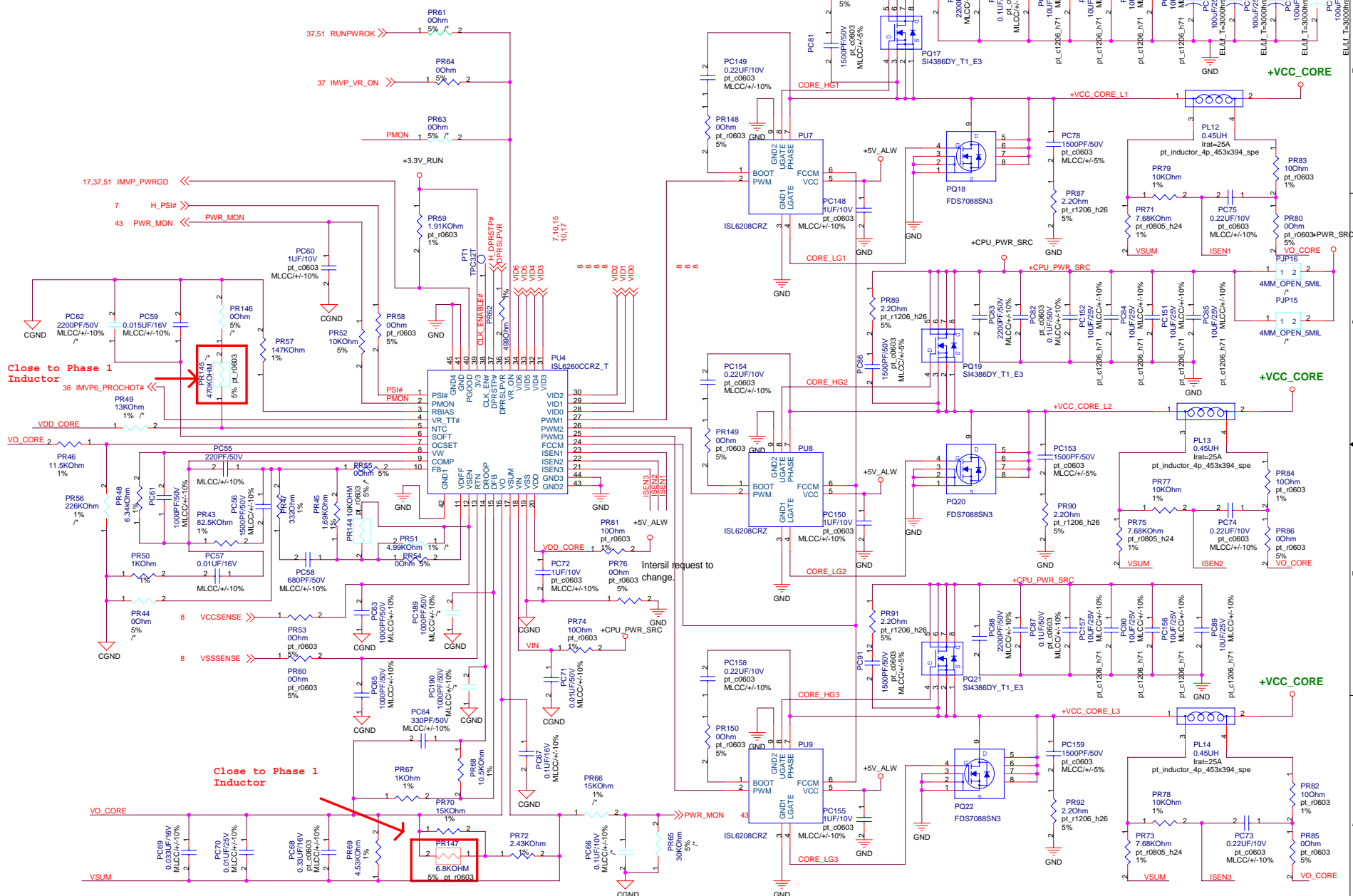
文才专用





PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: XDP	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: Terry Lin
	1.2	SHEET 52 OF 68			

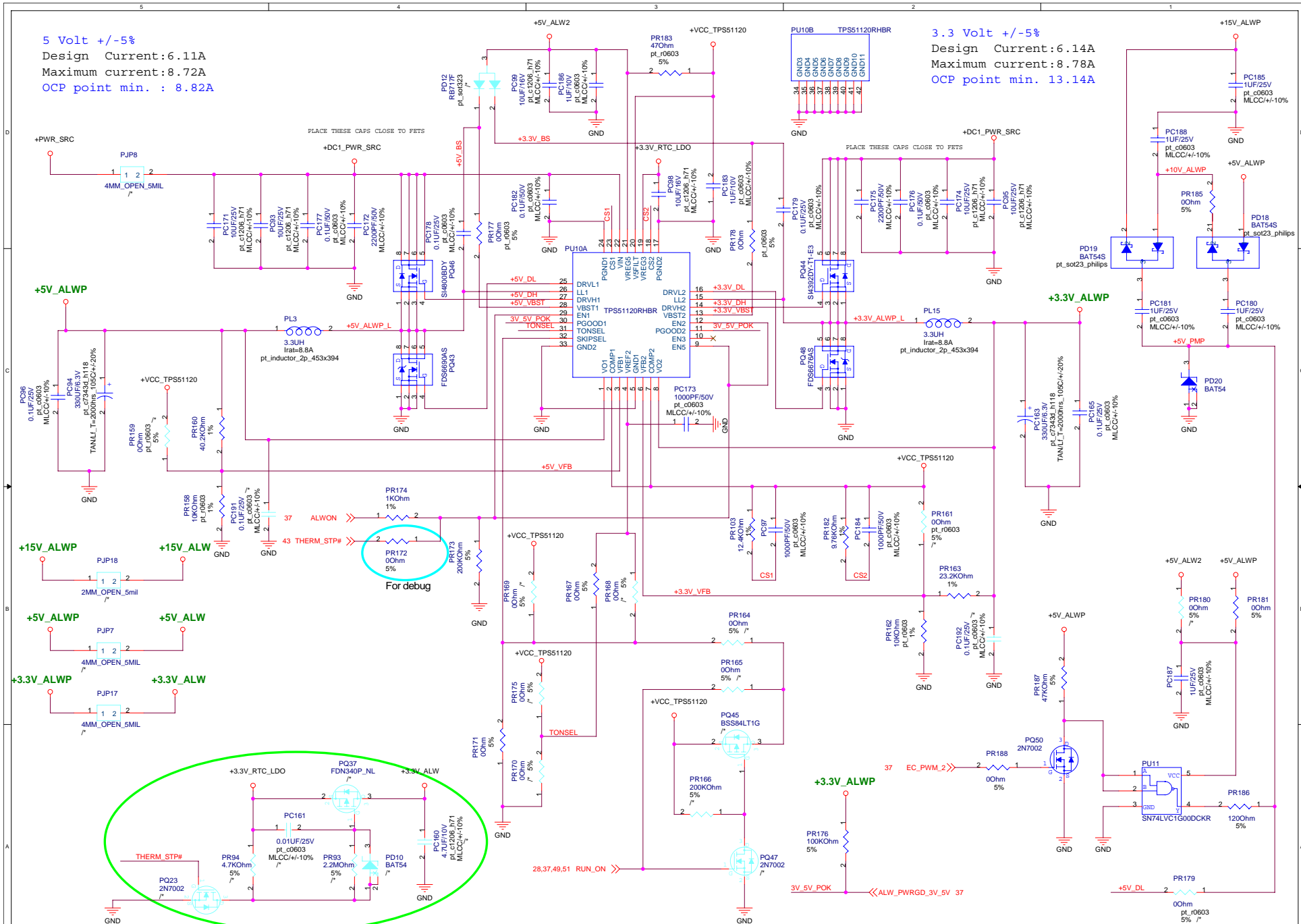
Design Current:35.2A
Maximum current:44A
OCP point min.50A



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: POWER_VCORE	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: JEFF
	1.2	SHEET 53 OF 68			

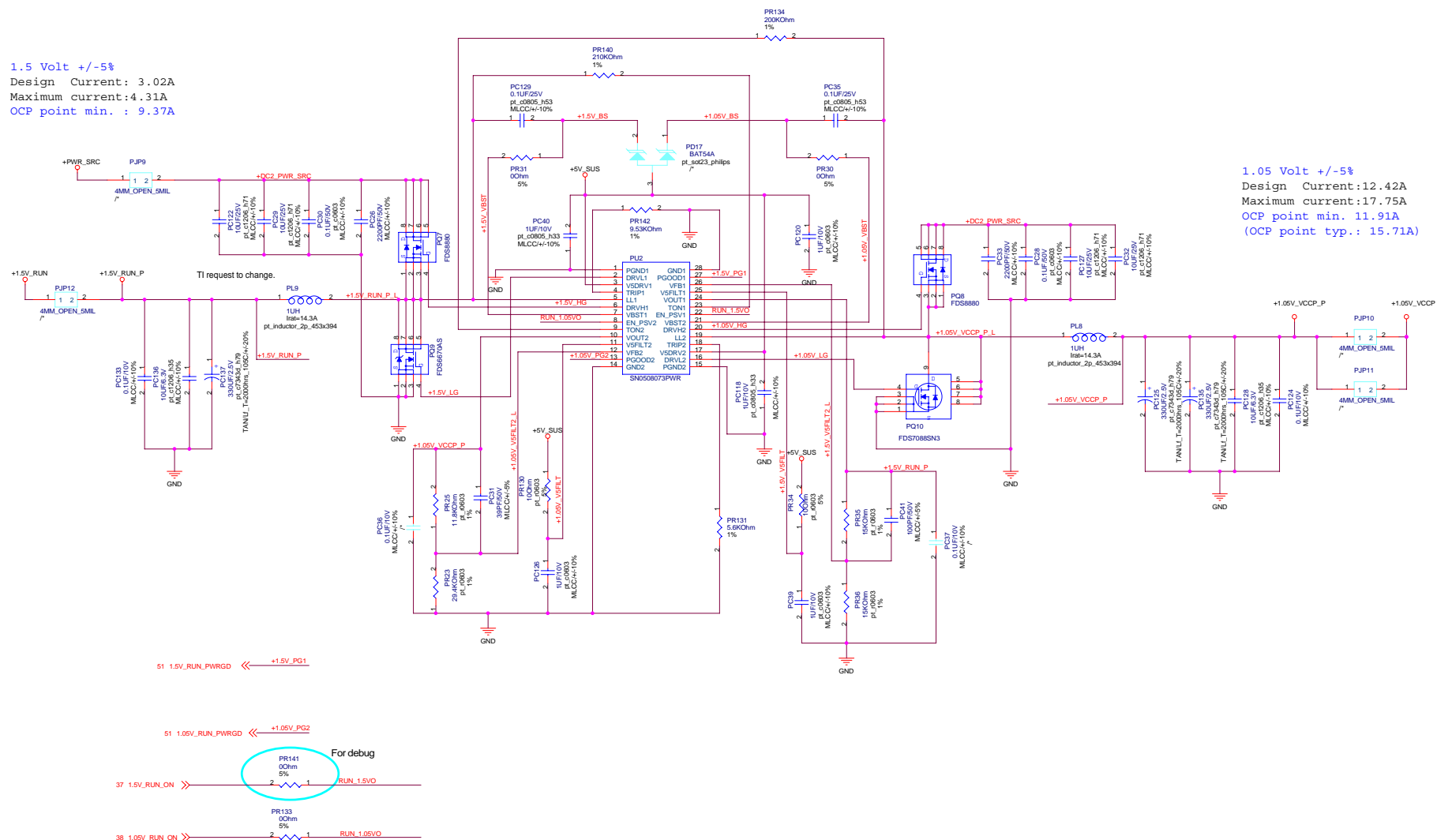
5 Volt +/-5%
Design Current:6.11A
Maximum current:8.72A
OCP point min. : 8.82A

3.3 Volt +/-5%
Design Current:6.14A
Maximum current:8.78A
OCP point min. 13.14A



PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: POWER_SYSTEM5V_ALW&3.3V_ALW	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : JEFF
	1.2	SHEET 54 OF 68		RELEASE DATE :		

1.5 Volt +/-5%
Design Current: 3.02A
Maximum current:4.31A
OCP point min. : 9.37A



1.05 Volt +/-5%
Design Current:12.42A
Maximum current:17.75A
OCP point min. 11.91A
(OCP point typ.: 15.71A)

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME:	<OrgName>	DESIGN ENGINEER:
	12	SHEET 55 OF 68	POWER I/O 1.5VS & 1.05VS	RELEASE DATE:		JEFF

TOTAL POWER=65W
-->3.34A

TABLE3 PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSOP
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
"NC" means no-connect		

Charge Current:4.68A
Discharge current:6.6A

TABLE2 MAXIM & INTERSIL BOM DIFFERENCES		
REF DES	MAXIM	INTERSIL
PR125	8.45K, 0402, 1%	16.0K, 0402, 1%
PC115	0.01uF	No Stuff
PC17	0.1uF, 0402, 10V	No Stuff
PC24	1.0uF, 0603, 10V	No Stuff
PR106	365K, 0402, 1%	215K, 0402, 1%
PR8	0, 0402, 5%	10, 0402, 5%
PR21	0, 0402, 5%	10, 0402, 5%
PC4	No Stuff	0.22uF
PC19	No Stuff	0.22uF
PC22	0.01uF	No Stuff
PC18	0.1uF, 0402, 10V	No Stuff
PC8	220pF, 0402, 50V	No Stuff
PD16	RB751V-40	No Stuff
PC13	3.3nF	No Stuff
PR19	1, 0603, 1%	0, 0603, 5%
PR9	100, 0402, 5%	0, 0402, 5%
PR22	4.7K, 0402, 5%	4.7K, 0402, 5%
PC23	0.01uF	0.01uF
PC21	0.01uF	0.01uF
PD3	1SS355	No stuff
PR12	1K, 0603, 5%	No stuff

TABLE1				
ADAPTOR (W)	TRIP CURRENT (A)	PR121	PR123	PR126 PR122
65	3.17	57.6K	13.0K	105 N/A
90	4.43	51.1K	17.8K	348 33.2K
130	6.43	32.4K	20.5K	100 27.4K
150	7.43	30.9K	24.9K	432 88.7K
200	9.75	19.1K	28K	301 36.5K
230	11.28	32.4K	6.49K	115 N/A

Note 1: PR122 is populated if ADAPT TRIP SET is used to program for the next lower adaptor
ADAPT TRIP SET is floating for the higher adaptor, grounded for the lower adaptor
Note 2: 24.9K at PR122 allows the 65W adaptor setting to switch down to 45W. (now is N/A)
Note 3: PR109 must be 5m ohm instead of 10m ohm for the 230W adaptor

PROJECT: Lanai

REVISION
1.2

DATE: Monday, March 19, 2007
SHEET 57 OF 68

DESCRIPTION: POWER CHARGER

SCHEMATIC FILE NAME: <OrgName>
RELEASE DATE:

DESIGN ENGINEER: JEFF

PROJECT: Lanai

REVISION

1.2

DATE: Monday, March 19, 2007

SHEET

59

OF 68

DESCRIPTION:

POWER_CONNECTOR

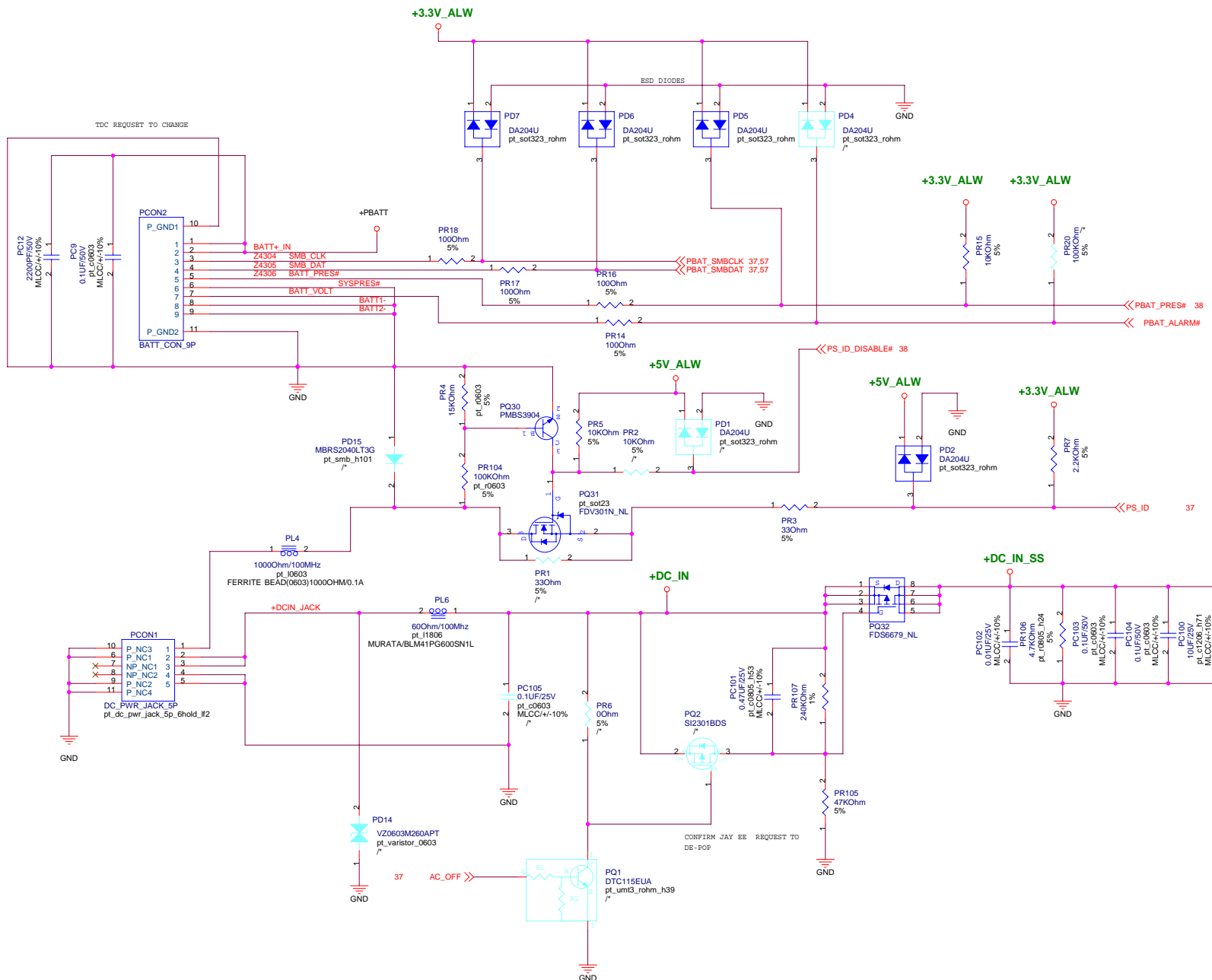
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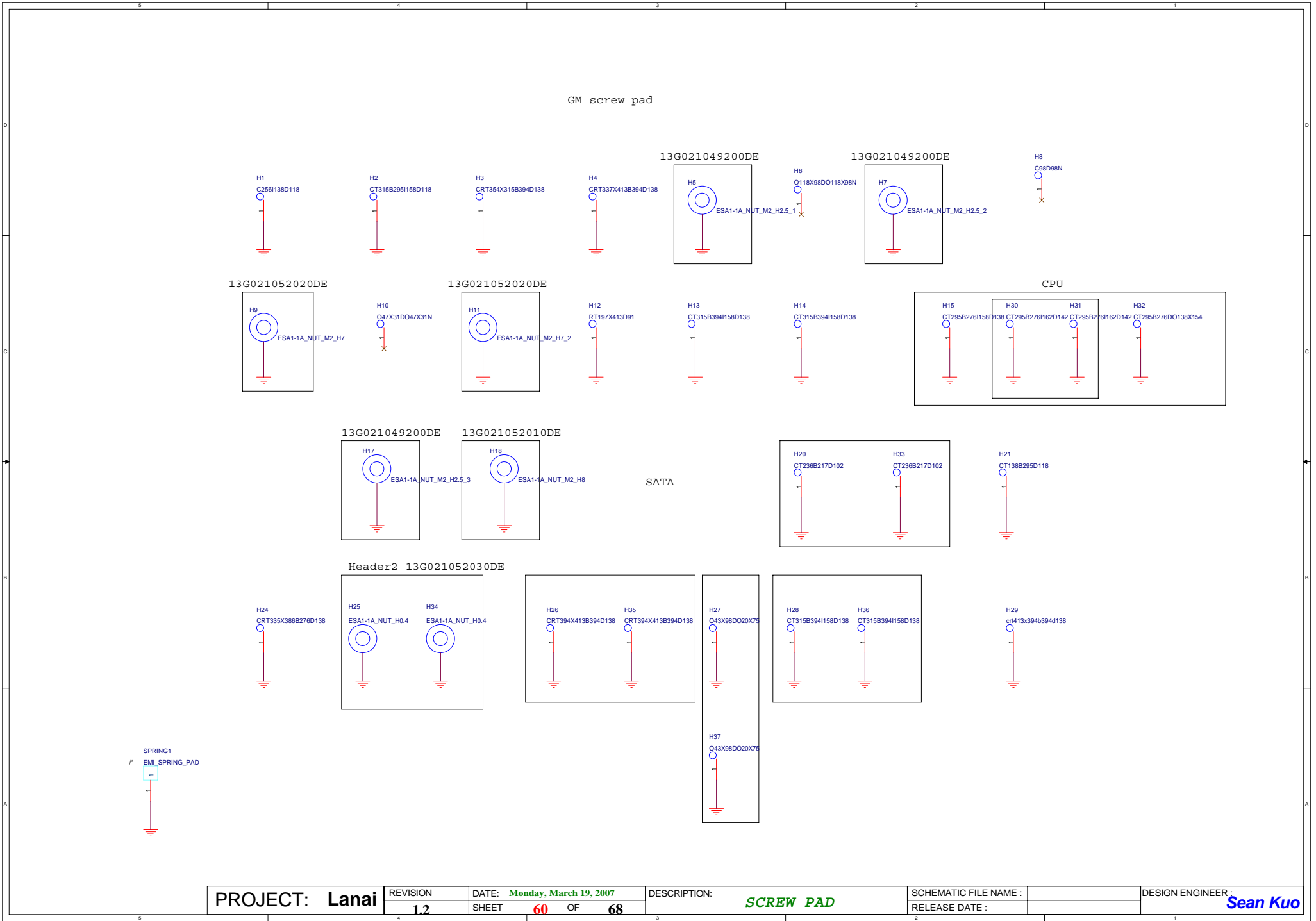
<OrgName>

DESIGN ENGINEER :

JEFF

RELEASE DATE :

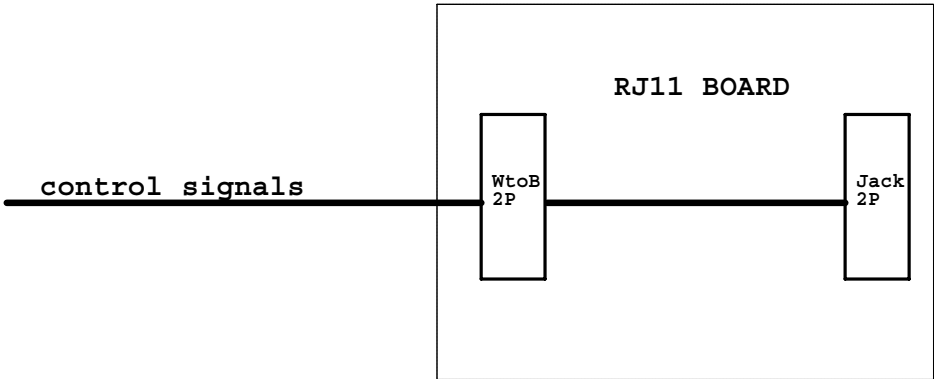




ASUS CONFIDENTIAL

MODEL NAME : *Elsa*

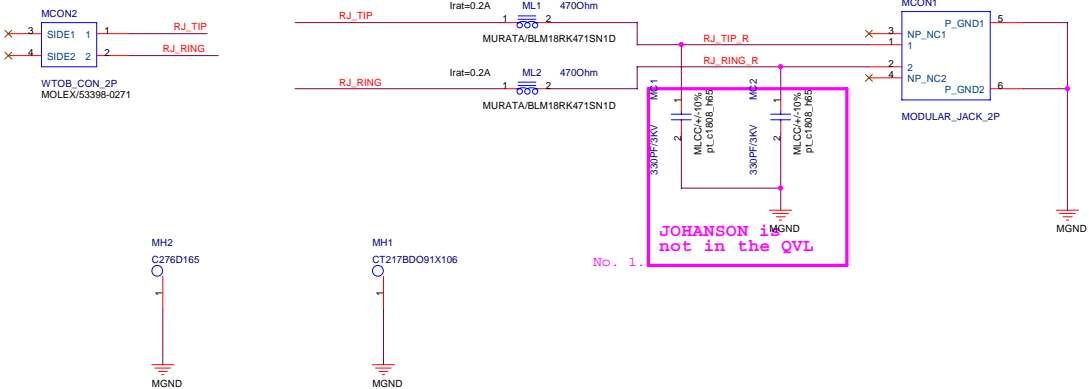
Lanai:Modem Board



REV : 1.1(DELL: X01)

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: <i>BLOCK DIAGRAM</i>	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 64 OF 68		RELEASE DATE :	

Stanly Hsu



No. 1.

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: RJ-11 CONN	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	1.2	SHEET 65 OF 68		RELEASE DATE :		Stanly Hsu

ASUS CONFIDENTIAL

MODEL NAME : *Elsa*

PCB NO : ???

ASUS P/N : ???

Lanai PP2 USB Board

REV : 1.1(DELL: X01)

MB PCB	
Part Number	Description
DA800004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???

PCB P/N: ???

PROJECT: **Lanai**

REVISION
1.2

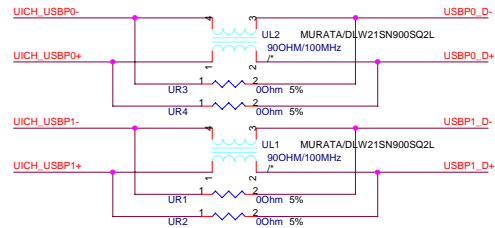
DATE: **Monday, March 19, 2007**
SHEET **67** OF **68**

DESCRIPTION: **Cover Page**

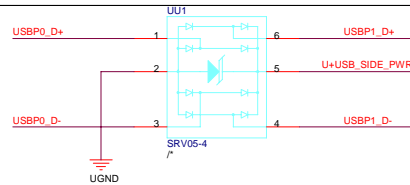
SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER :
Terry Lin

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

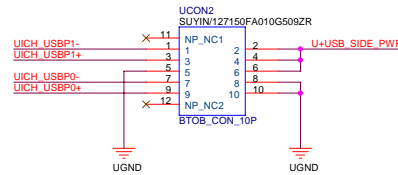


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

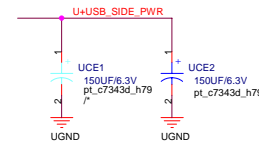


Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf) .

USB daughter board connector



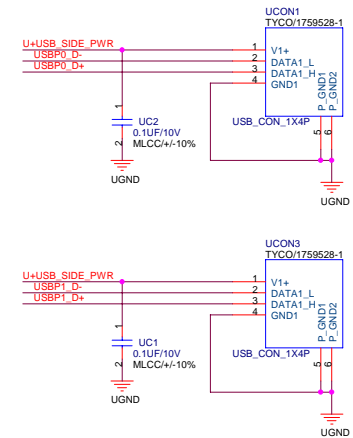
Place one 150uF cap by each USB connector



Each channel is 1A

Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines.
Add PADS ONLY until proven diodes are really needed.

Screw hole



PROJECT: Lanai

REVISION
1.2

DATE: Monday, March 19, 2007
SHEET 68 OF 68

DESCRIPTION:
USB PORT (SINGLE * 2)

SCHEMATIC FILE NAME :
RELEASE DATE :

<OrgName>

DESIGN ENGINEER :

Terry Lin